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Solid State Research

1981

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LEXINGTON, MASSACHUSETTS

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This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

SOLID STATE RESEARCH

QUARTERLY TECHNICAL SUMMARY REPORT

1 MAY - 31 JULY 1981

ISSUED 25 JANUARY 1982

LEXINGTON   MASSACHUSETTS

ABSTRACT

This report covers in detail the solid state research work of the Solid State
Division at Lincoln Laboratory for the period 1 May through 31 July 1981.
The topics covered are Solid State Device Research, Quantum Electronics,
Materials Research, Microelectronics, and Analog Device Technology.
Funding is primarily provided by the Air Force, with additional support
provided by the Army, DARPA, Navy, NASA, and DOE.

CONTENTS

INTRODUCTION

I. SOLID STATE DEVICE RESEARCH

Phase diagram analyses of the liquid-phase epitaxial (LPE) growth of $Hg_{1-x}Cd_xTe$ have been carried out to determine the interrelationships between growth solution composition, mercury vapor pressure, and growth temperature for various operational steps during the LPE growth cycle. The results indicate that it should be possible to grow good-quality epilayers of this material.

Carrier concentrations in the low 10^{16} cm^{-3} range and electron Hall mobilities over 10^5 cm^2/V-s at 77 K have been achieved in annealed LPE-grown $Hg_{1-x}Cd_xTe$ layers, with x in the 0.1 to 0.2 range. In the same range of x, the material constant that links layer thickness to growth time, number of degrees supercooling, and ramp rate has been determined to be approximately 0.75 μm/ C-min.$^{1/2}$.

A technique has been developed to monolithically integrate a passive waveguide with a GaInAsP/InP double-heterostructure laser for potential use in fabricating modulators and integrated external cavities. Initial tests of broad-area lasers with 400-μm passive waveguide sections showed threshold current densities of 2.4 to 3.1 kA/cm^2.

The feasibility of fabricating permeable-base transistors by molecular-beam epitaxial (MBE) growth of GaAs over tungsten gratings is being explored. By using a substrate temperature of 680 °C and an As_2/Ga ratio of 10, sufficient surface migration of the GaAs was achieved to permit the first single-crystal MBE growth of GaAs over amorphous tungsten gratings.

II. QUANTUM ELECTRONICS

A differential-absorption LIDAR (DIAL) system has been utilized to detect the exhaust pollutants (CO and C_2H_4) emitted by an A-10 jet aircraft at a range of 2.7 km. Concentrations of C_2H_4 were measured as the aircraft engines were started, run at fast idle, and shut down, with the greatest concentrations observed at shutdown. An increase in the concentration of CO was observed during engine startup and idle.

A pulse-pumped Co:MgF$_2$ laser, coded to 77 K, has generated up to 150 mJ of output energy per pulse and has been tuned between 1.596 and 2.288 μm, a 2000-cm^{-1} range. Room-temperature pulsed operation of a Ni:MgO laser, the first Ni:CAMGAR ($CaY_2Mg_2Ge_3O_{12}$) laser, and CW tunable laser action from V:MgF$_2$ have also been demonstrated. (See also Sec. III.)

The spectral width of CW, single-frequency GaAlAs diode lasers has been observed to saturate at high power levels due to refractive index fluctuations. These index fluctuations are thought to arise from electron number fluctuations in the small laser gain volume.

The electrical properties of single-crystal and amorphous Si, doped using a pulsed UV laser, have been studied as a function of laser wavelength and fluence, and of UV dose. Dissociation of molecules adsorbed on the Si surface can supplement photolysis of gas-phase molecules as a source of doping atoms.

An investigation of the properties of superconducting-insulator-superconducting (SIS) diodes in the submillimeter has been initiated using $Nb-Nb_2O_5-Pb$ devices fabricated on quartz. Mixing between the fifth harmonic of a 69-GHz klystron and a 345-GHz carcinotron yielded an IF with a 30-dB signal-to-noise ratio.

III. MATERIALS RESEARCH

Continuous single-crystal Si sheets over SiO_2 with areas of several square centimeters have been produced from polycrystalline Si films by two improved versions of the LESS technique (Lateral Epitaxy by Seeded Solidification) that use a composite Si_3N_4/SiO_2 encapsulating layer. N-channel MOSFETs fabricated in these films exhibit electron surface mobilities in the range of 600 to 700 $cm^2/V-s$, comparable to the values for devices fabricated in bulk Si.

Solid-phase epitaxial Si layers that are strongly p-type have been grown at 400 to 500°C by transport of Si atoms from an amorphous Si film through an Al film deposited on n-type Si substrates. This low-temperature process, which produces good rectifying junctions between the epitaxial layers and their substrates, has been used in the fabrication of solar cells with conversion efficiencies at AM1 of 10.4 and 8.5 percent on $\langle 100 \rangle$ Si and polycrystalline Si substrates, respectively, without an antireflection coating or back-surface field structure.

As part of a study of the lateral growth of InP layers over dielectric films by vapor-phase epitaxy, the rates of vertical growth by the $PCl_3-InP-H_2$ method on the four principal low-index planes have been determined as a function of substrate temperature for a source temperature of 700°C. For each substrate orientation, the growth rate exhibits a maximum between 620 and 660°C; up to 670°C, the rate increases in the order [111]B, [100], [111]A, and [110].

A theoretical model has been developed to describe the crystallization of a thin amorphous semiconductor film, supported on a thick substrate, that is irradiated by a heat pulse from a cylindrically symmetric energy beam. Solution of the integral equation for the dynamics of the amorphous-crystalline boundary radius yields three alternative types of motion — a series of jumps, a single longer jump, or indefinite runaway — that account for the structural features observed in pulsed-laser and electron-beam crystallization.

A gradient-freeze technique employing self-sealing graphite crucibles has been used to grow single crystals of MgF_2 doped with Ni, Co, or V, up to 3.7 cm in diameter and 10 cm long. High-quality laser rods up to 5 cm long have been fabricated from these crystals.

IV. MICROELECTRONICS

A charge-coupled device (CCD) implementation of a time-integrating correlator has been designed for use with the GPS (Global Positioning System) P-code which will require that the CCD be clocked at 20.46 MHz, or twice the P-code bit rate. The device uses a pipe-organ structure to achieve high-speed operation, and a complementary input structure to avoid signal- and code-dependent offsets.

A new CCD parallel-processing architecture has been developed which can perform many high-level mathematical functions such as vector-matrix, matrix-matrix, and triple-matrix products. The basic device consists of a floating-gate CCD tapped delay line and parallel arrays of CCD signal processors. All computations are performed in the charge domain, and each is the multiplication of a sampled analog data point with a digital word.

An optimized process for the high-resolution etching of aluminum on oxidized silicon wafers using a BCl_3 plasma has been developed. Constant plate-to-plate voltage and nonstandard system geometries have been used to achieve uniform etching with clean, vertical walls and no residues.

3200-$\overset{\circ}{A}$-period gratings, several-thousand-angstroms deep, have been etched in silicon using reactive-ion etching with an $Ar/SiCl_4/O_2$ gas mixture and aluminum or nickel as the etch mask material. Redeposition of SiO_2 during etching creates a keyhole cross section in the etched grooves when using an aluminum mask, and this phenomenon becomes more pronounced as the aluminum mask is made thicker.

Electron-beam techniques have been developed for defect location and adaptive interconnection on wafer-scale integrated systems. These techniques are compatible with a commercially available electron-beam lithography system and standard nMOS wafer processing. Test structures including an electron-beam multiplexer, floating-gate transistors, and simple FETs were designed, fabricated, and tested.

The feasibility of using integral microstrip transmission lines for interconnecting GaAs microwave devices has been demonstrated using a simulated mixer application. This fabrication technique, which employs a polyimide dielectric layer, permits direct electrical contact to the devices, and should substantially reduce the complex assembly procedures currently required by such devices.

V. ANALOG DEVICE TECHNOLOGY

A SAW delay line has been developed with very high (>100-dB) isolation between the short (10-ns) pedestal-of-delay acoustic signal and the direct electrical feedthrough signal by using edge-bonded transducers in a dual-track geometry. The high feedthrough isolation design provides the first practical means of providing high-performance SAW transversal filters with very short delay pedestal.

A comprehensive analysis has been made of the performance limits of integrated optical spectrum analyzers. Resolution is found to be limited to around 2.7 MHz and the time-bandwidth product to approximately 1000 with existing detector arrays. The aperture and weighting for the input lens are shown to be important with regard to resolution, crosstalk, and scalloping loss.

15 May through 15 August 1981

PUBLISHED REPORTS

Journal Articles

JA No.

5111	Infrared Spectroscopy Using Tunable Lasers	H. R. Schlossberg[*] P. L. Kelley	Chapter 4 in Spectrometric Techniques, G. A. Vanasse, Ed. (Academic Press, New York, 1981), Vol. 2, pp. 161-238
5129	A Comparison of Flash-Lamp-Excited $Nd_xLa_{1-x}P_5O_{14}$ (x = 1.0, 0.75, 0.20) Lasers	S. R. Chinn W. K. Zwicker[*]	J. Appl. Phys. 52, 66 (1981)
5131	$LiNbO_3$ Surface-Acoustic-Wave Edge-Bonded Transducers on ST Quartz and $\langle 001 \rangle$ Cut GaAs	D. E. Oates R. A. Becker	Appl. Phys. Lett. 38, 761 (1981)
5154	Optical Interferometric Measurement of the Thermal Expansion of NdP_5O_{14}	W. E. Barch S. R. Chinn W. K. Zwicker[*]	J. Appl. Phys. 52, 3388 (1981)
5165	UV Photolysis of van der Waals Molecular Films	D. J. Ehrlich R. M. Osgood, Jr.	Chem. Phys. Lett. 79, 381 (1981)
5166	Detectors for the 1.1 to 1.6 μm Wavelength Region	C. E. Hurwitz	Opt. Eng. 20, 658 (1981)
5168	Anodic Dissolution Technique for Preparing Large Area GaAs Samples for Transmission Electron Microscopy	J. P. Salerno J. C. C. Fan R. P. Gale	J. Electrochem. Soc. 128, 1162 (1981)
5174	Liquid-Phase Epitaxial Growth of InP and InGaAsP Alloys	S. H. Groves M. C. Plonko	J. Cryst. Growth 54, 81 (1981)
5175	Liquid-Encapsulated Czochralski Growth of InP Crystals	G. W. Iseler	J. Cryst. Growth 54, 16 (1981)
5176	Vapor-Phase Epitaxy of GaInAsP and InP	P. Vohl	J. Cryst. Growth 54, 101 (1981)
5185	Heteroepitaxy of Vacuum-Evaporated Ge Films on Single-Crystal Si	B-Y. Tsaur M. W. Geis J. C. C. Fan R. P. Gale	Appl. Phys. Lett. 38, 779 (1981)

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[*] Author not at Lincoln Laboratory.

MS No.

5428	TEM Investigation of the Micro-structure in Laser-Crystallized Ge Films	R. P. Gale J. C. C. Fan R. L. Chapman H. J. Zeiger	Proc. MRS Mtg. 1980: Defects in Semiconductors (North-Holland, New York, 1981), pp. 439-444
5429	Scanning Cathodoluminescence Microscopy of Polycrystalline GaAs	J. P. Salerno R. P. Gale J. C. C. Fan J. Vaughan*	Proc. MRS Mtg. 1980: Defects in Semiconductors (North-Holland, New York, 1981), pp. 509-514
5678	Liquid Phase Epitaxial Growth of $Hg_{1-x}Cd_xTe$ from Te-Rich Solutions	T. C. Harman	Proc. SPIE Vol. 285: Infrared Detector Materials (Society of Photo-Optical Instrumentation Engineers, Bellingham, Washington, 1981), pp. 84-91

UNPUBLISHED REPORTS

Journal Articles

JA No.

5186	Solid-Phase Epitaxial Crystal-lization of Amorphous Ge on $\langle 100 \rangle$ Si	B-Y. Tsaur J. C. C. Fan J. P. Salerno C. H. Anderson R. P. Gale F. M. Davis E. F. Kennedy* T. T. Sheng*	Accepted by J. Electrochem. Soc.
5218	Efficient Si Solar Cells by Low-Temperature Solid-Phase Epitaxy	B-Y. Tsaur G. W. Turner J. C. C. Fan	Accepted by Appl. Phys. Lett.
5240	Improved Techniques for Growth of Large-Area Single-Crystal Si Sheets over SiO_2 Using Lateral Epitaxy by Seeded Solidification	B-Y. Tsaur J. C. C. Fan M. W. Geis D. J. Silversmith R. W. Mountain	Accepted by Appl. Phys. Lett.
5243	Ultrathin, High-Efficiency Solar Cells Made from GaAs Films Prepared by the CLEFT Process	C. O. Bozler R. W. McClelland J. C. C. Fan	Accepted by IEEE Electron Device Lett.
5245	Mixing of 10 μm Radiation in Room Temperature Schottky Diodes	P. E. Tannenwald H. R. Fetterman C. Freed C. P. Parker B. J. Clifton R. G. O'Donnell	Accepted by Opt. Lett.
5247	Remote Probing of the Atmo-sphere Using a CO_2 DIAL System	D. K. Killinger N. Menyuk	Accepted by IEEE J. Quantum Electron.

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* Titles of Meeting Speeches are listed for information only. No copies are available for distribution.

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I. SOLID STATE DEVICE RESEARCH

A. THEORY OF THE LPE GROWTH OF $Hg_{1-x}Cd_xTe$ LAYERS

In order to use the liquid-phase epitaxial (LPE) technique for $Hg_{1-x}Cd_xTe$, phase diagram analyses are required. A useful starting point for phase diagram analysis is Gibbs' phase rule, which states that

$$F = C - P + 2 \quad,$$

where F is the number of degrees of freedom, C the number of components, and P is the number of phases. For the ternary HgCdTe system, there are 3 components and also 3 phases, since all 3 components are relatively volatile at modest temperatures; therefore $F = 2$, and there are available two degrees of freedom which can be used to fix both the temperature, T, and the total vapor pressure, P, and thereby attain a compositionally stabilized solution for LPE growth. The total vapor pressure is the sum of the partial pressures of the 3 components,

$$P = P_{Hg} + P_{Cd} + P_{Te_2} \quad;$$

however,

$$P_{Hg} \gg P_{Te_2} \quad or \quad P_{Cd} \quad.$$

Therefore, for a particular temperature, it is possible to choose a partial vapor pressure of Hg and a liquid composition of $(Hg_{1-z}Cd_z)_{1-y}Te_y$ such that a changing composition which is relatively constant with respect to time can be attained in an open-tube configuration for Te-rich HgCdTe alloy solutions. Consequently, one can anticipate the growth of good quality LPE layers.

In order to understand the physical processes within the growth tube during the growth cycle, considerations of the vapor-liquid-solid phase relations are a necessity. In Fig. I-1 are shown the two pertinent phase diagrams, i.e., the liquidus temperature vs atomic fraction Te and the partial pressure of Hg vs reciprocal temperature. The diagram in Fig. I-1(a) can be related to the temperature and composition of the growth solution, whereas the diagram in Fig. I-1(b) can be related to a Hg reservoir temperature (ordinate) and the growth solution temperature (abscissa). If a growth solution is saturated and is in equilibrium with Hg vapor, then the conditions described by point A in Figs. I-1(a) and -1(b) occur. The partial Hg vapor pressure P_{Hg} is equal to the three-phase equilibrium partial pressure of Hg denoted by P_E. Also, the liquid would be in equilibrium with solid $Hg_{1-x}Cd_xTe$ at point S, if solid is present. If the Hg pressure is raised above P_E as indicated in Fig. I-1(b), then $P_{Hg} > P_E$ and Hg atoms are absorbed into the growth solution. As a result, the liquidus composition changes in the direction of point B, as indicated in Fig. I-1(a). As Hg is absorbed, the growth solution becomes first a supercooled liquid (if no solid is present initially), and then a two-phase mixture of liquid and solid. The melting point of the mixture becomes greater than the melting point of the original saturated solution. Also, the atomic fraction of Cd in the solution and mixture decreases, i.e., $z_B < z_A$. Similarly, if the Hg pressure is lowered below P_E as indicated by the A to C arrow in Fig. I-1(b), then Hg evaporates from the growth solution, which produces changes in the melting point and the composition of the growth solution, as indicated in Fig. I-1(a), i.e., in the direction of under-saturation or a lowered melting point and an increased atomic fraction of Cd, $z_C < z_A$.
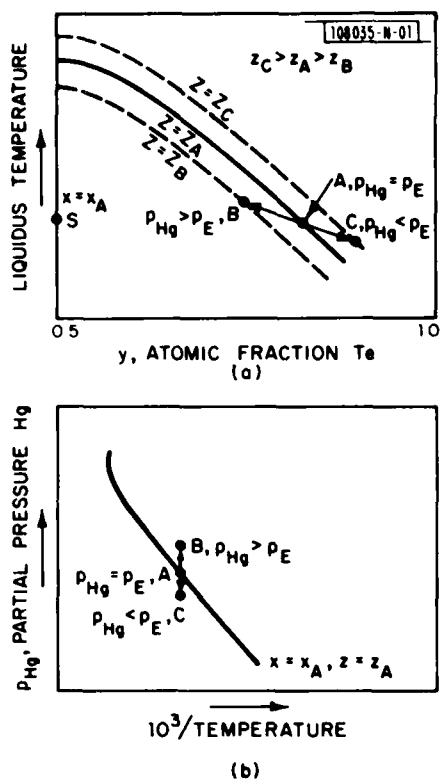
Fig. I-1. Schematics of (a) liquidus temperature vs atomic fraction Te of $(Hg_{1-z}Cd_z)_{1-y}Te_y$ and (b) partial pressure of Hg vs reciprocal temperature of $(Hg_{1-z}Cd_z)_{1-y}Te_y$.
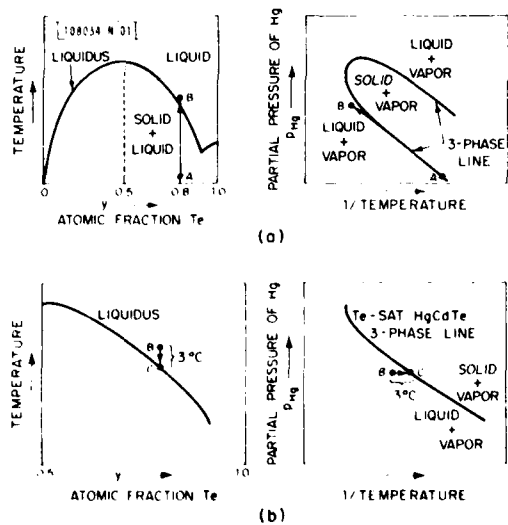
Fig. I-2. Schematics of (a) growth solution and Hg reservoir temperature changes superimposed on the relevant phase diagrams during heat-up prior to LPE growth and (b) growth solution temperature changes prior to equilibration of the growth solution with the Hg vapor at the liquid-vapor interface and the source wafer at the solid-liquid interface.
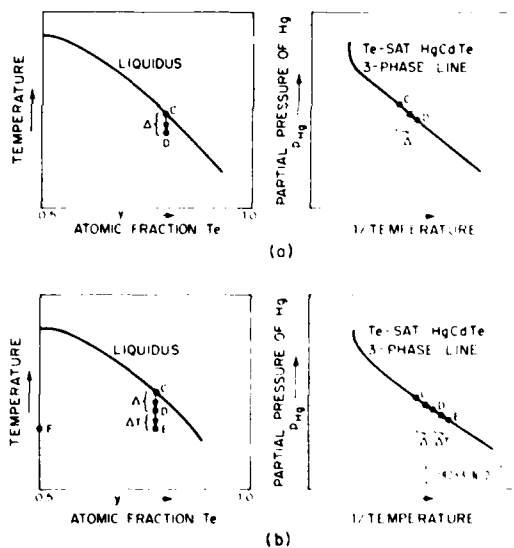
Fig. I-3. Schematics of (a) growth solution and Hg reservoir temperature changes for the step-cooling growth mechanism and (b) temperature changes for the growth solution and Hg reservoirs for the supercooling growth mechanism.

2

Figures I-2 and -3 show relevant phase diagrams for HgCdTe along with operational steps for LPE growth. Figure I-2(a) displays schematically the growth solution temperature and Hg pressure or Hg reservoir temperature changes superimposed on the relevant phase diagrams for the heat-up part of the growth cycle, whereas Fig. I-2(b) shows schematically growth solution and Hg reservoir temperature changes prior to equilibration of the growth solution with the Hg vapor at the liquid-vapor interface and the CdTe source wafer at the solid-liquid interface. Initially, the growth solution is heated from room temperature to about 3°C above the liquidus line as indicated by the A to B arrow. Simultaneously, the Hg in the Hg reservoir is heated to a temperature such that the Hg partial pressure at the growth solution-Hg vapor interface falls slightly below the three-phase line as indicated by point B. After the complete dissolution of the quenched ingot material in the growth solution reservoir, the temperature of the growth solution is lowered 3°C as indicated in Fig. I-2(b). At point C, the growth solution is very nearly a saturated solution. The source wafer is placed under the growth solution and the equilibration temperature is maintained for 60 min., which is long enough to insure formation of a homogeneous growth solution that is saturated by contact with the source wafer and is equilibrated with the proper Hg vapor pressure as indicated by point C in Fig. I-2. In Fig. I-3(a) is portrayed a schematic diagram of the growth solution and Hg reservoir temperature changes for the step-cooling growth mechanism. Similar changes are given for the supercooling mechanism in Fig. I-3(b). For growth, the source wafer is moved away from the growth bin and cooling is begun. Growth is initiated by bringing the substrate into contact with the growth solution at supercoolings of typically 2° to 10°C. Further cooling is discontinued. For the step-cooling mechanism, the cooling rate is continued so that an appreciable additional contribution to the layer thickness occurs due to continued cooling (D to F in the diagram). Note that the Hg reservoir temperature is changed so that the Hg vapor pressure follows the three-phase line. Growth is terminated by moving the substrate away from the growth solution.

<div align="right">T. C. Harman</div>

B. $Hg_{1-x}Cd_xTe$ LPE GROWTH PARAMETERS AND CHARACTERIZATION DATA

Over the past two decades there has been an increasing interest in $Hg_{1-x}Cd_xTe$ for practical applications as well as fundamental studies. Homogeneous, nearly perfect single crystals of $Hg_{1-x}Cd_xTe$ have been difficult to prepare primarily because of the high vapor pressure of mercury at the melting points of the various stoichiometric compositions of interest. To overcome this problem, a new liquid-phase-epitaxial (LPE) growth system[1-4] has been designed. The new method involves generating a Hg vapor stream over the growth solution using a two-temperature zone system.[3] One zone controls the solution temperature while the other controls the Hg pressure over the solution. This open-tube, horizontal-slider system has been used extensively for the growth of LPE layers of $Hg_{1-x}Cd_xTe$ from Te-rich $(Hg_{1-z}Cd_z)_{1-y}Te_y$ (y = 0.8, typically) alloy growth solutions in the 450° to 496°C temperature range.

In Table I-1 some typical LPE growth parameters and characterization data are given. The typical growth temperature range is 496 to 488°C. Although the data of the right-hand column of Table I-1 suggest only a trend, more extensive measurements over a wider range of Hg boat temperatures indicate the sensitivity of the run-to-run dependence of alloy composition on the Hg boat temperature (for constant growth solution temperature) during the 1-hr equilibration phase of the growth cycle, i.e., higher Hg boat or reservoir temperature correlates with a lower

TABLE I-1

(a) SOME LPE GROWTH PARAMETERS

Run No.	Cooling Rate, R_G (°C/min.)	Growth Time, t (min.)	Degrees of Supercooling, Δ (°C)	Growth Temperature Range (°C)	Equilibration Temperature of Hg Boat (°C)
151	2.7	1.0	10	450–447.3	–
893	0.28	30	2	496–488	276.2[*]
894	0.28	30	2	496–488	276.4
895	0.28	30	2	496–488	276.2
896	0.28	30	2	496–488	276.0

(b) SOME CHARACTERIZATION DATA

Run No.	Substrate Area (mm^2)	Layer Thickness, d (μm)	Transmission Cutoff, λ_c (μm)	Mole Fraction (CdTe, x)
151	4 × 10	7	–	0.205 ± 0.003[†]
893	8 × 8	30	6.8	0.187 ± 0.024
894	8 × 8	33	7.6	0.165 ± 0.028
895	8 × 8	32	7.2	0.168 ± 0.007
896	8 × 8	30	5.9	0.219 ± 0.035

[*] For static conditions, Hg boat temperature would be ~260°C (from Ref. 5).

[†] No inhomogeneity detected, since estimated error limit of electron microprobe is ±0.003.

CdTe content of the alloy and vice versa, in agreement with theory. The transmission cutoff wavelength, λ_c (for 1-percent transmission), correlates satisfactorily with the mole fraction of CdTe in the layers.

Run No.	Growth Time, t (min.)	Layer Thickness, d (μm)	LPE Layer Anneal* Temperature (°C)	Hg Boat Anneal* Temperature (°C)	Mole Fraction (CdTe, x)	Carrier Concentration (cm^{-3}, 77K)	Carrier Mobility (cm^2/V-s)
845	10	5	–	–	0.168 ± 0.029	8.6×10^{15}	9.7×10^4
883	10	10	250	250	0.147 ± 0.019	1.3×10^{17}	7×10^4
884	10	7	350	250	0.140 ± 0.018	$4.1 \cdot 10^{16}$	4.3×10^4
896	30	30	250	250	0.219 ± 0.035	1.0×10^{16}	6.1×10^4
904	30	18	250	275	0.125 ± 0.026	2.1×10^{16}	1.4×10^5
906	30	20	275	275	0.196 ± 0.006	1.0×10^{16}	1.0×10^5
908	30	40	250	250	0.121 ± 0.015	3.0×10^{16}	2.8×10^5

TABLE I-2

ADDITIONAL CHARACTERIZATION DATA

*Anneal times 1 hr.

Table I-2 exhibits additional characterization data. Layer thicknesses are in the 5- to 40-μm range. After in situ annealing, the carrier concentrations of the layers are typically in the low 10^{16} cm^{-3} range with more recent runs yielding carrier mobilities over 10^5 cm^2/V-s at 77K. The unusually high electron mobilities indicate that the layers are of high quality. Growth solution sizes in the 2.0- to 10-g range have been investigated, but no significant effect of melt size on electrical properties has been observed.

In Fig. I-4, the layer thickness, d, is plotted for various growth times, t. Data are presented for HgCdTe layers grown by both the step-cooling and the supercooling techniques for x = 0.2. For a supercooled solution being further cooled by ramping, the layer thickness d relationship[6] is given as

$$d = C(\Delta t^{1/2} + \frac{2}{3} R_G t^{3/2}) \tag{I-1}$$

where C is the material constant, Δ is the degrees supercooling, R_G is the cooling rate during growth, and t is the growth time. By fitting the experimental data to the d vs t equation, the material constant C is found to be 0.7 μm/°C-min.$^{1/2}$. The growth of the epilayers is initiated at a growth temperature T_G of about 496°C with cooling rates R_G of 0 and 0.28°C/min. for the step-cooling and supercooling techniques, respectively. In the step-cooling experiments,

Fig. I-4 (left graph)

CALCULATED, $d = C(\Delta t^{1/2} + 2/3\, R t^{3/2})$, $C = 0.7\, \mu m/°C \cdot min^{1/2}$
○ EXPERIMENTAL DATA, $\Delta \simeq 2°C$, $R_G = 0.28\, °C/min$
△ EXPERIMENTAL DATA, $\Delta \simeq 2°C$, $R_G = 0$
□ EXPERIMENTAL DATA, $\Delta \simeq 14°C$, $R_G = 0$
$T_G = 496°C$
$X = 0.2$

STEP-COOLING

SUPERCOOLING – GROWTH MECHANISM

STEP-COOLING GROWTH MECHANISM

d, GROWTH THICKNESS (μm)

t, GROWTH TIME (min)

108051-N-01

Fig. I-5 (right graph)

CALCULATED $d = C \Delta t^{1/2}$ WHERE $C = 0.8\, \mu m/°C \cdot min^{1/2}$
○ EXPERIMENTAL DATA, $\Delta = 10°C$, $R_\Delta = 0.7\, °C/min$
$T_G \sim 496°C$
$X = 0.1$

STEP-COOLING GROWTH MECHANISM

d, GROWTH THICKNESS (μm)

t, GROWTH TIME (min)

108050-N-01

Fig. I-4. Layer thickness vs growth time for $Hg_{0.8}Cd_{0.2}Te$ layers grown by the step-cooling and supercooling growth techniques.

Fig. I-5. Layer thickness vs growth time for $Hg_{0.9}Cd_{0.1}Te$ layers grown by the step-cooling growth technique.

Fig. I-6 graph

WAVELENGTH (μm)

TEMPERATURE = 295 K

108029-N

LPE-906, $X = 0.196 \pm 0.006$

LPE-908, $X = 0.121 \pm 0.015$

PERCENT OPTICAL TRANSMISSION

WAVE NUMBER (cm^{-1})

Fig. I-6. Percent optical transmission vs wave number and wavelength for two LPE layer-substrate composites.

6

2° and 14°C of supercooling were used. The cooling rates for supercooling R_Δ were 0.67°C/min. and 0.28°C/min. for the step-cooling and supercooling techniques, respectively. In Fig. I-5, d vs t data are shown for x = 0.1, T_G = 496°C, R_Δ = 0.67°C/min., R_G = 0, and Δ = 10°C. It is seen that the experimental data are in satisfactory agreement with Eq. (I-1) for C = 0.8 μm/ °C-min.$^{1/2}$.

For each epitaxial layer, optical transmission measurements were made on the layer-substrate composite with a double-beam spectrophotometer having a light-spot area of 25 mm^2. In Fig. I-6 the percent transmission is plotted against wave number and wavelength for two representative layers with CdTe mole fractions of 0.121 and 0.196, as determined by electron microprobe analysis. The photon cutoff wavelength for run 906 is in good agreement with the literature value[7] for this composition. The sharpness of the absorption edge is consistent with good depth and lateral homogeneity.

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A. E. Paladino

C. LPE GROWTH OF INTEGRATED GaInAsP/InP LASER AND PASSIVE WAVEGUIDE

Monolithic integration of passive waveguides with double heterostructure (DH) lasers has the potential for a number of interesting device applications, including lasers with distributed Bragg reflectors or integrated external cavities, intensity or frequency modulators, and mode-locked DH lasers. Previous attempts to achieve this structure with the GaAs/GaAlAs system, however, resulted in high waveguide loss, high laser threshold current density, and difficulties with control of the liquid-phase-epitaxial (LPE) growth procedures.[8-12] We have developed a new LPE technique to grow $Ga_{x_2}In_{1-x_2}As_{y_2}P_{1-y_2}$/InP DH passive waveguides integrated with and precisely aligned to previously grown $Ga_{x_1}In_{1-x_1}As_{y_1}P_{1-y_1}$/InP DH laser structures. Uniform waveguide layers and good surface morphology have been achieved in the LPE regrowth. Relatively low threshold current densities (2.4 to 3.1 kA/cm^2) were obtained in a preliminary test of broad area lasers with one integrated passive waveguide section.

The fabrication procedure is illustrated in Fig. I-7. Oxide stripes of 500-μm width on 1250-μm centers were first fabricated on a previously grown DH laser wafer. The unprotected sections of the InP cap layer were removed by etching in HCl, after which the oxide mask was removed. To dissolve the sections of the $Ga_{x_1}In_{1-x_1}As_{y_1}P_{1-y_1}$ (Q_1) layer exposed by the HCl etch, two different selective etchants have been used in separate experiments: (1) an aqueous solution of $K_3Fe(CN)_6$ and KOH, and (2) a mixture of H_2O, H_2SO_4 and H_2O_2 (10:1:1 in volume). After the removal of the unprotected Q_1 layer, the sample was dipped in 70°C KOH solution and buffered HF, each for 1 min., and was then immediately loaded into an LPE system with pre-baked graphite slider and growth solutions. The LPE system was purged with a mixture of PH_3 and purified H_2, while being heated to 670°C. After approximately 60 min., the system was then cooled to the growth temperature (636°C) in a 10-min. interval. The sample was first slid under the quaternary solution for 10 to 60 s for the growth of the $Ga_{x_2}In_{1-x_2}As_{y_2}P_{1-y_2}$ (Q_2) layer, and then under an InP growth solution for 2 to 10 min. The energy band gap of the Q_2 alloy was 1.03 eV, while that of the Q_1 alloy was 0.95 eV.

Figure I-8 shows the scanning electron micrographs of the cleaved and stained cross sections of two as-grown samples [(a) and (b)] in which No. 1 and 2 Q-etchants, respectively, were used in the pre-LPE processing. The Q_2 layers show discontinuities at the mesa edges, similar

(a) DOUBLE HETEROSTRUCTURE LASER WAFER

OXIDE MASK

p-InP CAP LAYER

Q₁ ACTIVE LAYER

n-InP BUFFER LAYER

n-InP SUBSTRATE

(b) SELECTIVE CHEMICAL ETCHING

(c) LPE REGROWTH AND DEVICE FABRICATION

Au-Zn

InP (UNDOPED)   OXIDE   Zn-DIFFUSED

Q₂ WAVEGUIDE   Q₁

CLEAVED MIRROR   Au-Sn   CLEAVED MIRROR
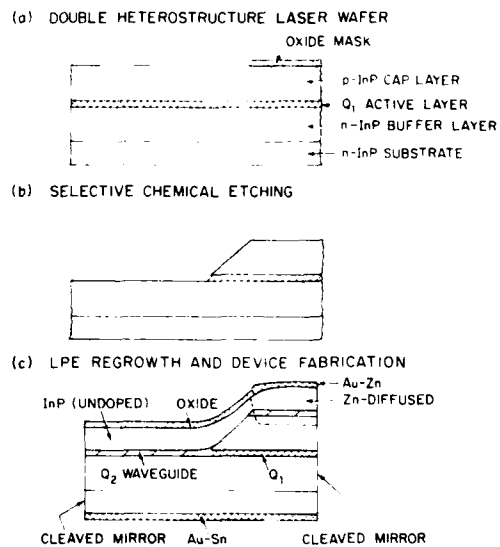
111492-N

Fig. I-7.   Processing steps for the monolithic integration of a passive
waveguide to a GaInAsP/InP DH laser.

Fig. I-8. Scanning electron micrographs
of the cross sections of two samples in
which a DH passive waveguide has been
grown integrated with a GaInAsP/InP
laser. Different growth features of Q_2
layers were related to different etchants
used in the pre-LPE processing.
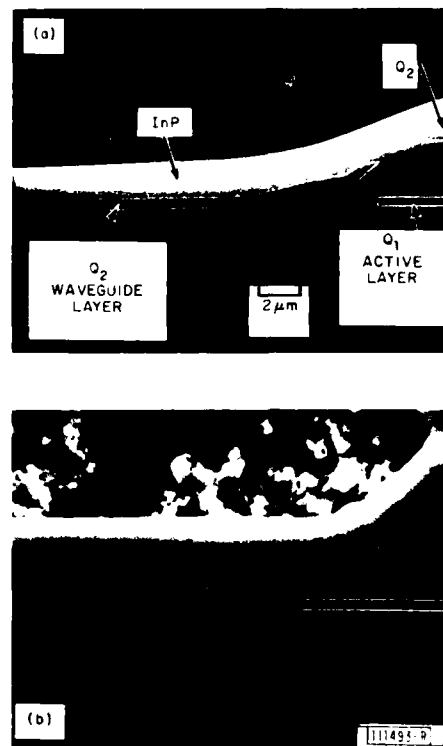
to that observed by Kishino et al. in their fabrication of mesa-substrate buried heterostructure
lasers.[13] As evident in Fig. I-8(a), the Q_2 waveguide layer tended to grow thicker near the
waveguide-laser junction. This was found to be related to the shape of the mesa edge formed
by the undercutting in the Q_1-layer etching and subsequent vapor-phase migration of In just
before the LPE regrowth. This effect was less pronounced in samples treated by No. 2 Q-etchant
which had produced less undercutting [Fig. I-8(b)]. Good surface morphologies [Fig. I-9(a)] have
been obtained with high reproducibility for samples treated by No. 1 Q-etchant. In these samples,
the Q_2 waveguide layers were generally uniform, smooth, and continuous, with very occasional
disruptions. However, samples treated by No. 2 Q-etchant contained many discontinuities in the
regrown waveguides, and good surface morphology has not yet been achieved [Fig. I-9(b)].

One sample with all necessary doping concentrations was grown for initial laser testing.
In this particular wafer, the Q_2 waveguide layer was fairly thick (1.5 μm near the waveguide-
laser junction and 1.0 μm for the rest) compared to the Q_1 active layer (0.3 to 0.4 μm). Broad-
area lasers with one integrated passive waveguide section 200 to 350 μm in length and laser sec-
tion 350 to 440 μm in length showed threshold current densities of 2.4 to 3.1 kA/cm^2, which were
~40 percent higher than those of control lasers cleaved from the same wafer but without the inte-
grated waveguides (J_{th} = 1.7 to 2.4 kA/cm^2).

One possible cause of the somewhat higher threshold current density is the coupling loss
due to the mismatch in thickness between the waveguide and the laser active layer. With im-
proved coupling and a thinner laser active layer, lower threshold can likely be achieved.

LASER   WAVEGUIDE   LASER
SECTION   SECTION   SECTION

200 μm

(a)

(b)
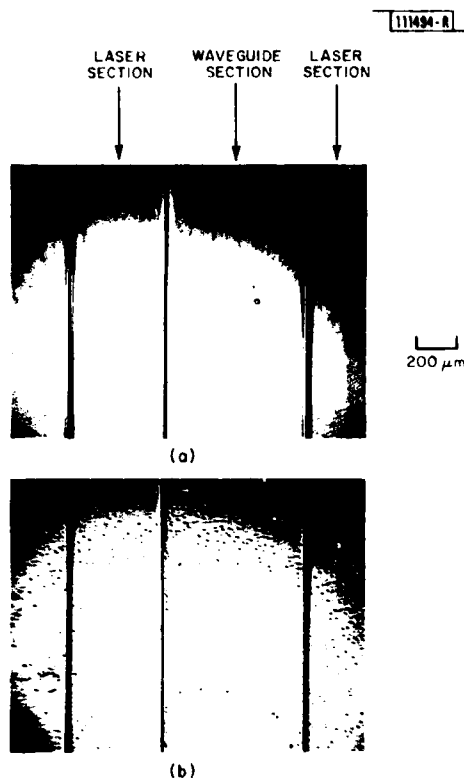
Fig. I-9. Nomarski optical micrographs of the surfaces of two different samples after the LPE regrowth of waveguide layers. Difference in surface morphologies was related to different etchants used in the pre-LPE processing.

Furthermore, the layer uniformity and good surface morphology achieved in this work should make future fabrication of stripe-geometry devices possible.

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J. N. Walpole

D. MBE GROWTH OF GaAs OVER TUNGSTEN GRATINGS

One of the crucial steps in the fabrication of the permeable-base transistor (PBT) is the overgrowth of the metal grating with crystalline device-quality semiconductor material. The experiments described here are being carried out to determine the feasibility of using molecular-beam-epitaxial (MBE) growth of GaAs over tungsten gratings to achieve this structure.

Several GaAs substrates were covered with a tungsten fan pattern with line widths and spacings of several micrometers. The substrate surfaces were oriented in the (100) direction, tilted 2° to 5° toward the ⟨111⟩ axis, and were similar to the substrates used in vapor epitaxial growth. The tungsten was deposited by electron beam evaporation and was amorphous. The fan pattern in the tungsten layer provided a complete set of tungsten lines in all azimuthal orientations, so that any directional dependence for lateral overgrowth could be observed. Initial growth conditions were those previously used for MBE growth of GaAs, i.e., a substrate temperature at 580°C, an As_2/Ga ratio of 1, and a growth rate of 1 μm/hr. Cracked arsine was used for the arsenic source.[14] The system consequently had a hydrogen background pressure of 1×10^{-6} Torr. Under these conditions nucleation occurred both on and between the tungsten lines. As has been

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reported[15] for growth over amorphous SiO_2, the GaAs was polycrystalline over the amorphous tungsten and single crystal over the GaAs. It was noted, however, that the growth rate was lower over the tungsten and that crystal facets were formed along the edges of the tungsten lines, indicating that the sticking coefficient of GaAs is lower on tungsten than on GaAs and that some surface migration is taking place near the tungsten line edges. The faceting did not seem to depend on azimuthal orientation. To enhance surface migration, which would be evidenced by the formation of larger facets, both the substrate temperature and As_2/Ga ratio were increased. At a substrate temperature of 680°C and an As_2/Ga ratio of 10, faceting occurred not only along the tungsten lines but over the GaAs as well, and the faceting was clearly perpendicular to the tilt direction. The growth was repeated on a similar GaAs substrate without the tungsten pattern, and the resulting surface morphology is shown in Fig. I-10. The almost perfect staircase-like structure in the tilt direction is believed to be a classical example of the Kossel-Stranski model[16]

Fig. I-10. SEM micrograph of the surface morphology of a GaAs epitaxial layer grown at 680°C by MBE on a (100) GaAs substrate tilted 5° toward the ⟨111⟩ direction.

(a)

(b)
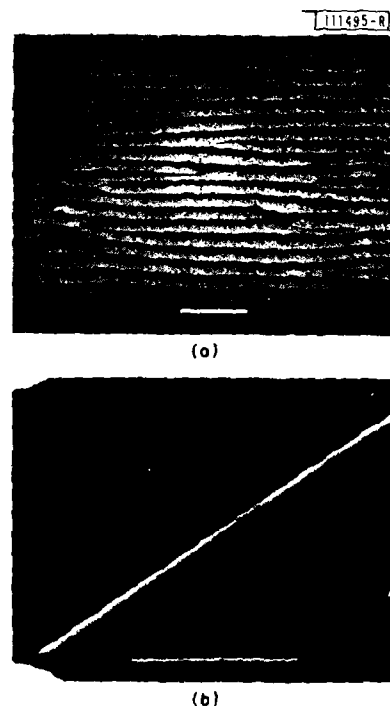
of crystal growth, as shown in Fig. I-11. According to this model, atoms or molecules migrate easily over the terraces and are more tightly bound at the ledges or kink sites. Normally these steps occur only on an atomic scale and cannot be seen. However, if the migration lengths are increased and the substrate is tilted off from the (100) plane by a few degrees, one might expect the steps to be more pronounced. This type of terrace growth has also been observed in the liquid-phase-epitaxial growth of GaAs (Ref. 17). The step widths (~2 μm) are comparable to average migration distances of Ga-As pairs on a (100) GaAs substrate.
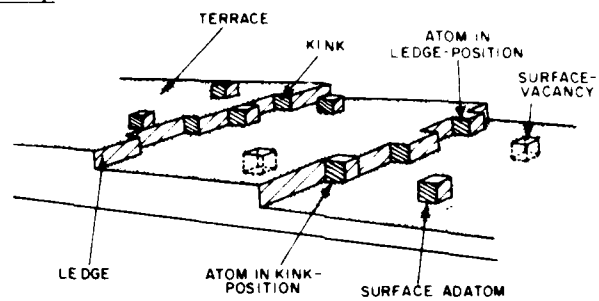
Fig. I-11. Kossel-Stranski model of crystal surfaces.
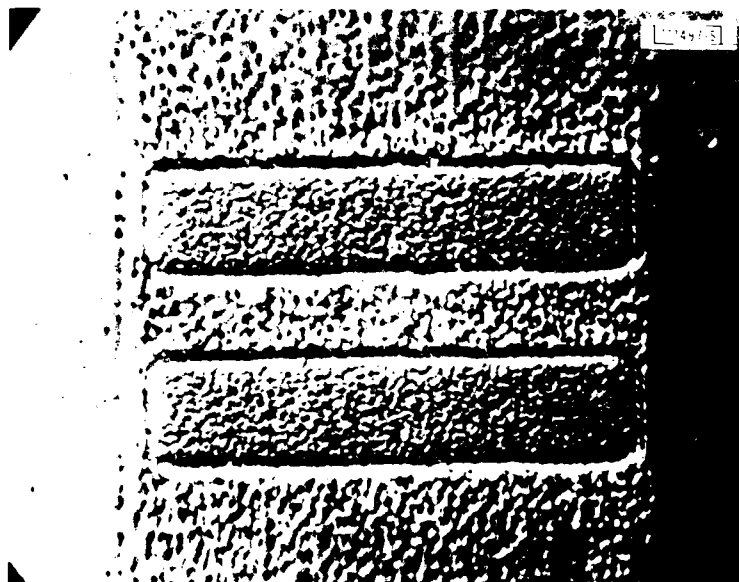
Fig. I-12. Interference contrast microphotograph of MBE overgrown tungsten gratings and contact pads. Magnification is 1040X.

After it had been shown that lateral migration of GaAs over GaAs for distances of several micrometers could take place during MBE growth, overgrowth of submicrometer tungsten lines was attempted. A tungsten grating 400-$\overset{\circ}{A}$ thick with a 3200-$\overset{\circ}{A}$ periodicity and a line-to-space ratio of unity was used. The GaAs substrate was oriented in the (100) plane with a 5° tilt toward the $\langle 11 1 \rangle$ "A" direction, and the grating lines were oriented 10° off the tilt direction and hence 10° from the normal to a cleavage plane. A series of pairs of tungsten contact pads, each pad having dimensions of 10 × 50 μm with 10-μm separation between paired pads and 180-μm separation between pair centers, was then placed on the surface with the 50-μm dimension of the pads perpendicular to the grating lines. The result of the first attempt to overgrow this structure with GaAs by MBE is shown in Fig. I-12, which is an interference contrast photograph of the region around one pair of pads. The grating extends over the entire wafer surface and, except for the areas near the pads, is smoothly overgrown. The tungsten pad areas are well defined in the overgrowth because of a difference in surface morphology and because the grown layer is significantly thinner over the pads. The morphology is considerably poorer between the contact pads, which seem to affect the quality of the GaAs overgrowth either through strain effects or contamination. A scanning electron microscope view of a cleaved cross section of this structure is shown in Fig. I-13. Because the contact pads and grating lines are oriented 10° from the cleavage plane, several of the grating lines between the pads intersect the cleaved surface. The rough cleaves over the contact pads on the left and right sides of Fig. I-13 are indicative of the polycrystalline growth over the pads. The smooth cleave over the grating in the center of the picture is indicative of single-crystal growth. The GaAs MBE layer is 0.7 μm thick between the pads and 0.5 μm over the pads, indicating a lower sticking coefficient for GaAs on tungsten and/or a higher surface mobility, which causes the GaAs to build over the crystalline areas. The buildup of GaAs at the pad edges also supports this hypothesis.
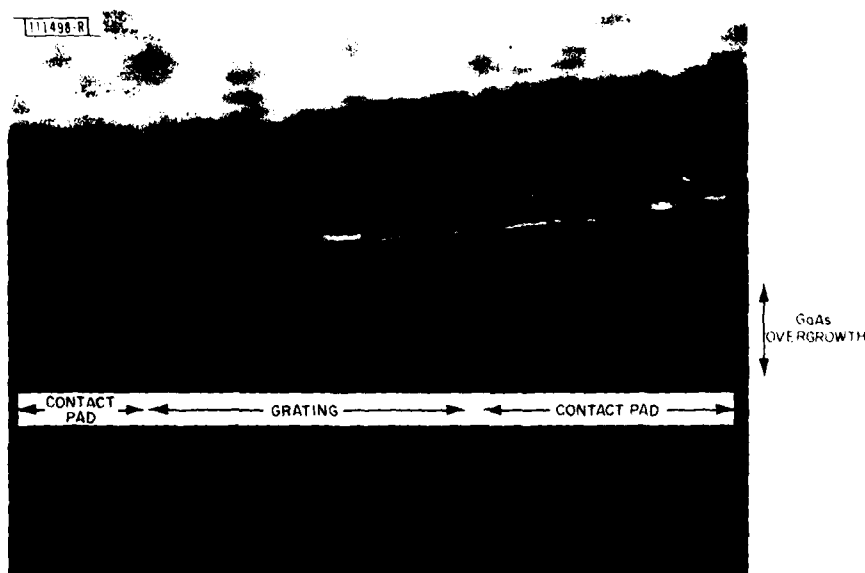
Fig. I-13. SEM micrograph of a cleaved cross section of GaAs MBE overgrowth of tungsten contact pads (right and left sections) and of a tungsten grating (center section).

The GaAs substrate orientations used in these experiments were chosen to be the same as those used for vapor epitaxial overgrowth. The facet orientation of this MBE growth at 680°C suggests that grating orientations more nearly normal to the tilt direction may be preferred.

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17. See, for example, E. Bauser, M. Frik, K. S. Loechner, L. Schmidt, and R. Ulrich, J. Cryst. Growth $\underline{27}$, 148 (1974); also D. L. Rode, J. Cryst. Growth $\underline{27}$, 313 (1974).

II. QUANTUM ELECTRONICS

A. LASER REMOTE SENSING OF A-10 JET AIRCRAFT EXHAUST

The dual-CO_2-laser differential-absorption LIDAR system[1] of the Lincoln Laboratory Remote Sensing Facility has been used to detect the presence of CO and C_2H_4 in the exhaust gases emitted by an A-10 jet aircraft located 2.65 km from the facility. These measurements utilized backscattered radiation from several targets behind the aircraft at a range of 2.7 km. The aircraft was situated approximately 15 m upwind from the LIDAR beam and the initial flow direction of the A-10 exhaust plume was perpendicular to the LIDAR beam direction. Temporal changes in the concentration of C_2H_4 were measured as the tethered A-10 started its engines, operated at a fast idle, and turned its engines off. This was followed by similar measurements of the changing concentration of CO in the atmosphere as the A-10 engine was restarted and increased its speed prior to departure.

Results for ethylene (C_2H_4) are shown in Fig. II-1. As seen, the measured path-averaged background concentration of C_2H_4 was approximately 2 to 5 ppb. Increases in the C_2H_4 concentration on the order of 5 ppb were observed when the A-10 started its engines; larger increases were evident when the engines were turned off.

Figure II-2 shows the results for CO. Each point given in the figure represents a running average of the concentration over approximately a 2-min. interval. The results shown indicate an average increase over the 2.7-km range on the order of 100 ppb due to A-10 exhaust emission. The unusually high background CO concentration of about 400 ppb observed over the airfield hampered the sensitivity of the measurement by greatly increasing the absorption of the on-resonance backscattered return; the background concentration of CO is normally on the order of 100 to 200 ppb.

The above results may be compared with those predicted from knowledge of the exhaust effluent of the A-10 aircraft. The concentrations at idle speed from an A-10 are approximately[2] 400-ppm meter for CO and 15-ppm meter for C_2H_4, with a reduction in CO concentration at faster engine settings; in addition, the cross-sectional mass concentration of the exhaust plume is fairly constant over a range of 10 to 20 m behind the A-10 (Ref. 2). Under these approximations, and assuming an initial laser beam/exhaust plume interaction length of 1 m, one calculates that the expected increase in the C_2H_4 concentration over the integrated 2700-m range should have been (400-ppm meter/2700 m) ~ 5 ppb. Similarly, the expected increase of CO should have been approximately 150 ppb. These results are consistent with the measured increases observed in Figs. II-1 and -2.

<div align="right">

D. K. Killinger
N. Menyuk

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B. ADVANCES IN TRANSITION-METAL LASERS

A series of experiments has been carried out to characterize the operation of $Ni:MgF_2$, $Ni:MgO$, $Ni:CaY_2Mg_2Ge_3O_{12}$ (CAMGAR) and $Co:MgF_2$ lasers under conditions of pulsed optical excitation. Highlights of the results include attainment of a normal-mode output of 150 mJ per pulse at 1.92 μm from a $Co:MgF_2$ laser and demonstration from the same device of a continuous tuning range from 1.596 to 2.288 μm. In addition, room-temperature operation of the $Ni:MgO$ laser has been obtained along with the first laser operation of $Ni:CAMGAR$.
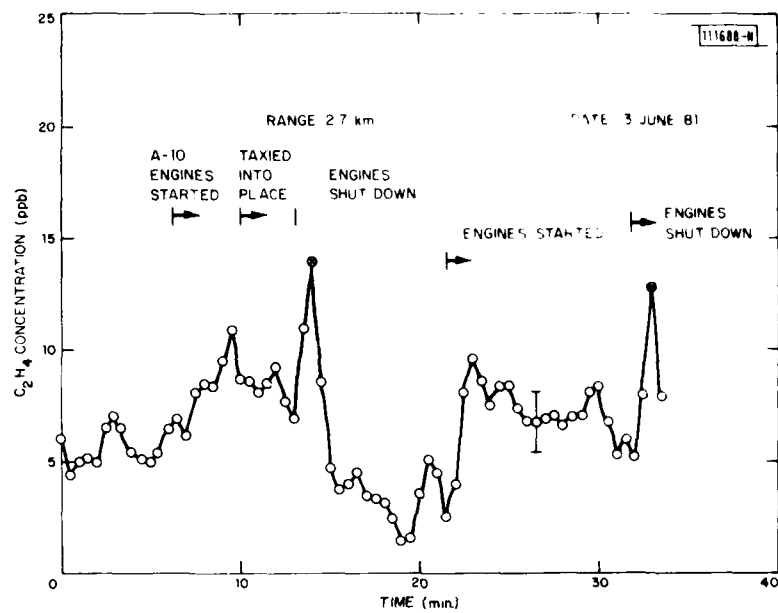
Fig. II-1. Laser remote detection of C_2H_4 from the exhaust of an A-10 jet aircraft located at a range of 2.7 km.
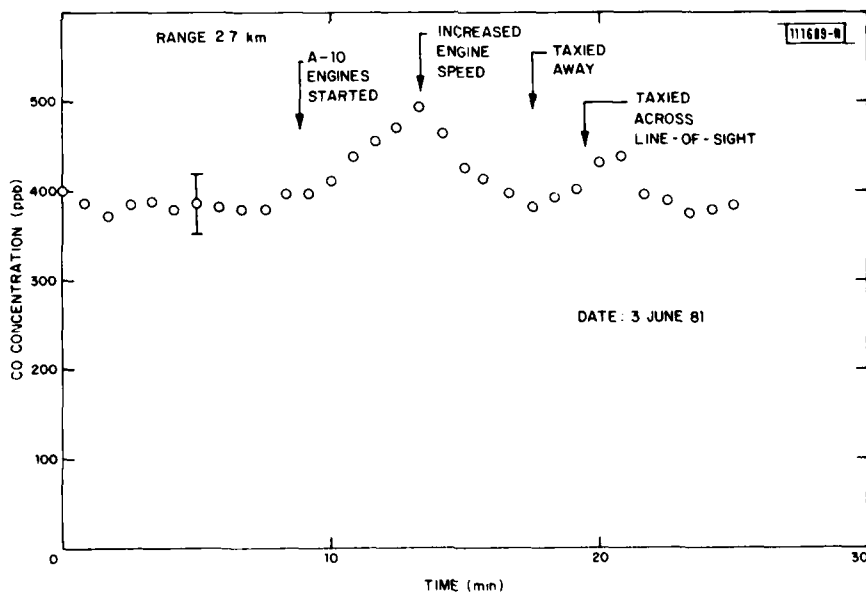
Fig. II-2. Laser remote detection of CO from the exhaust of an A-10 jet aircraft located at a range of 2.7 km.

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Research in V^{2+}-doped crystals has resulted in the first demonstration of CW operation of a V:MgF$_2$ laser (tunable from 1.07 to 1.16 μm) and in measurement of the absorption and fluorescence properties of V:MnF$_2$.

The pulsed excitation source employed in the experiments with Ni^{2+} and Co^{2+} lasers was a flashlamp-pumped Nd:YALO laser capable of generating output pulses of up to 650 mJ in energy and ~1 ms in duration at a wavelength of 1.34 μm. In addition, operation at up to 750 mJ of output energy per pulse at 1.08 μm was possible by changing cavity optics. The configuration of the transition-metal lasers was similar to that described previously.[3] The majority of measurements were carried out with a pump-laser repetition rate of 4 Hz and with the crystals cooled to liquid-nitrogen temperature.

Fig. II-3. Output energy vs input energy for 1.2-cm-long crystals of Ni:MgF$_2$ and Co:MgF$_2$.
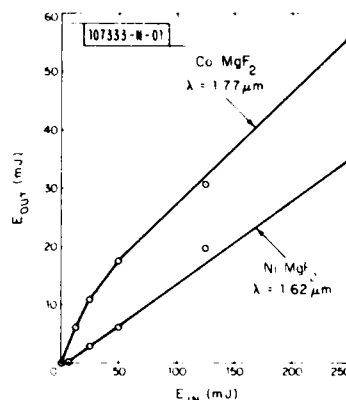
Figure II-3 shows the input-output curves of Ni:MgF$_2$ and Co:MgF$_2$ lasers employing Brewster-angle crystals 1.2 cm in length. The Ni:MgF$_2$ and Co:MgF$_2$ crystals absorbed, respectively, 75 and 50 percent of the incident pump energy; the ratio of output coupling to total cavity loss was similar for both lasers. Taking these factors in account, one can calculate that at high pumping levels the Co:MgF$_2$ laser quantum efficiency is 2.5 times greater than that of the Ni:MgF$_2$ laser. It is possible that absorption of the pump radiation by a transition from the first excited state ($^3T_2$) to a higher level ($^3T_1$) of Ni^{2+} causes a reduction in the Ni:MgF$_2$ laser efficiency. Further research is required to confirm this hypothesis.

The input-output performance of a Co:MgF$_2$ laser constructed with a 2.7-cm-long Brewster crystal is shown in Fig. II-4. There was no tuning element in the laser cavity; the three output wavelengths shown in the figure were obtained by use of different sets of cavity mirrors. A conversion efficiency from input to output energy of up to 25 percent was demonstrated. The quantum efficiency of the laser, calculated on the basis that 46 percent of the pump energy was absorbed in the crystal, was 79 percent at 1.92 μm. Average output power vs pump repetition rate at a pump input energy of 400 mJ is shown in Fig. II-5. At a 25-Hz rate the laser output power was initially 2.5 W and then dropped after several seconds to 2.2 W, indicating a slow rise in laser crystal temperature. Improved heatsinking techniques should allow full output energy at rates up to the ~50 Hz limit of the pump laser. The tuning curve for the Co-MgF$_2$ laser (Fig. II-6) was generated by insertion of a single-plate birefringent tuning element in the cavity. Both the short- and long-wavelength limits of the tuning range may be possibly extended by proper choice of laser mirror coatings.
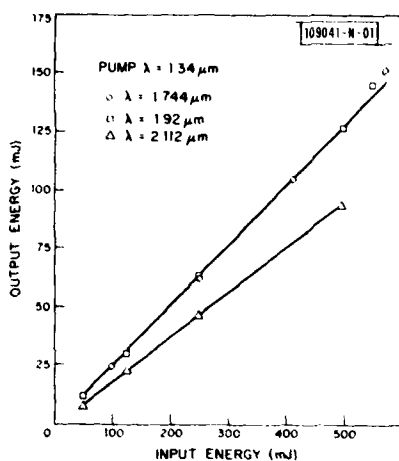
Fig. II-4. Output energy vs input energy for a 2.7-cm-long Co:MgF$_2$ crystal at three different operating wavelengths.
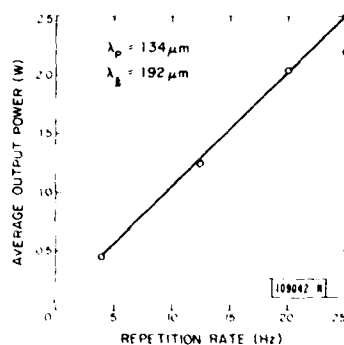
Fig. II-5. Average output power vs pulse repetition rate for Co:MgF$_2$ laser at an input energy of 400 mJ.
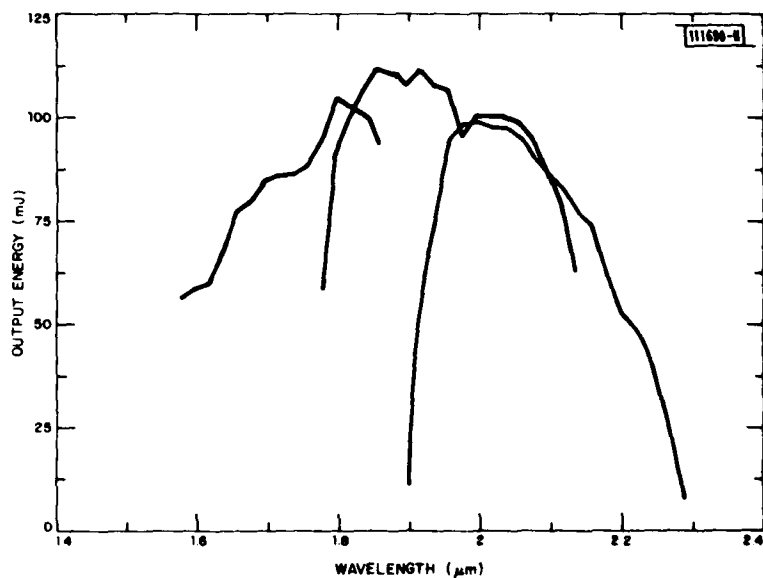
Fig. II-6. Tuning curves of Co:MgF$_2$ laser, obtained with three different sets of cavity mirrors.

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Operation of a Ni:MgO laser under pulsed 1.08-μm excitation was examined. The laser crystal was the same one used in previous experiments.[3] At liquid nitrogen temperature the threshold was ~2 mJ, and up to 125 mJ of output energy at 1.316 μm was obtained at a quantum efficiency of ~60 percent. Ni:MgO has been considered as a possible medium for room-temperature operation because of minimal temperature quenching of the $^3T_2 \rightarrow {}^3A_2$ fluorescence.[4] Operation of the pulsed Ni:MgO laser at crystal temperatures above 80 K was observed by removing the liquid nitrogen from the dewar and allowing the temperature to rise slowly. The laser output energy vs temperature curve is shown in Fig. II-7 for an input energy of 250 mJ. At 180 K the laser wavelength shifted to 1.37 μm. At 293 K the threshold was 310 mJ and operating wavelength was 1.378 μm.
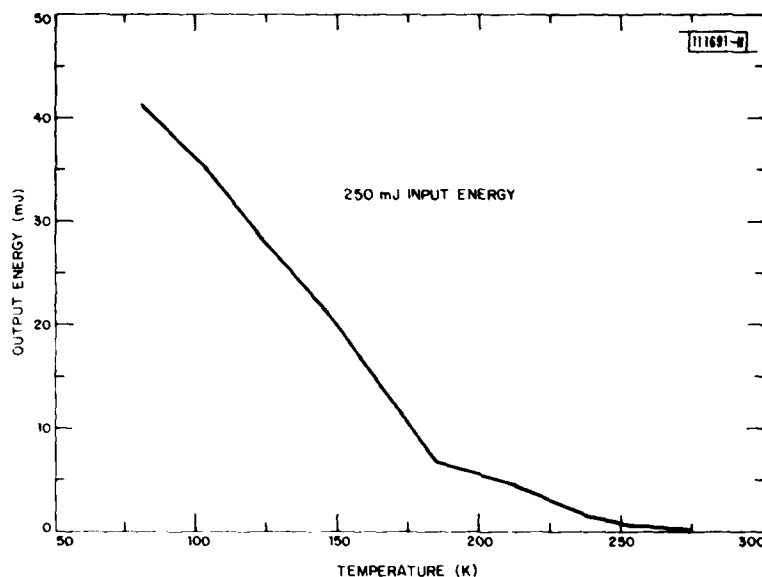
Fig. II-7. Output energy of Ni:MgO laser vs crystal temperature for an input energy of 250 mJ.

Some of the fluorescence properties of Ni:CAMGAR have been reported previously.[5] Laser operation of liquid-nitrogen-cooled Ni:CAMGAR was observed at 1.46 μm under pulsed 1.08-μm excitation. The 0.6- × 0.6- × 2.8-cm laser crystal[6] had flat and parallel, AR-coated end surfaces. The output vs input curves for the Ni:CAMGAR laser (Fig. II-8) show both much higher thresholds and lower slope efficiencies than for the other transition-metal lasers described above. The relatively small change in threshold with output coupling indicates a high level of internal loss in the laser. Determining whether or not such relatively poor performance is an intrinsic property of Ni:CAMGAR will require additional spectroscopic studies.

A CW V:MgF$_2$ laser has been operated in the 1.1-μm wavelength region. The laser cavity configuration was similar to that used in operation of the tunable, CW Ni:MgO laser.[3] The optical pumping source was a CW argon-ion laser operating on the 0.5145-μm line which provided excitation of the $^4A_2 \rightarrow {}^4T_1$ transition. The Brewster-angle laser crystal was doped with
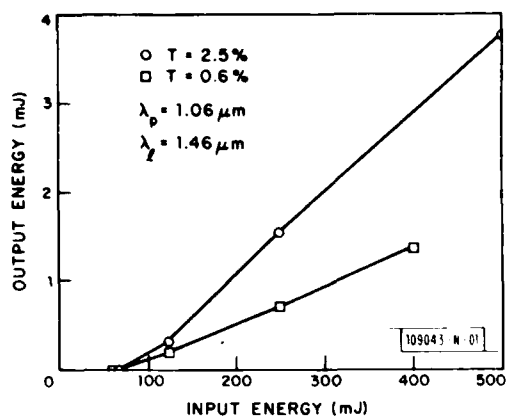
Fig. II-8. Output energy vs input
energy of Ni:CAMGAR laser for
two different coupling mirrors.
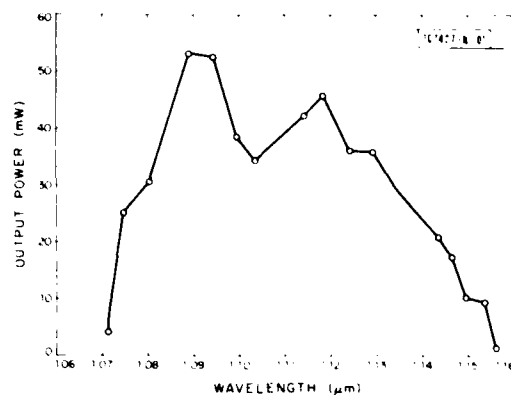
Fig. II-9. Tuning curve of CW V:MgF$_2$ laser.
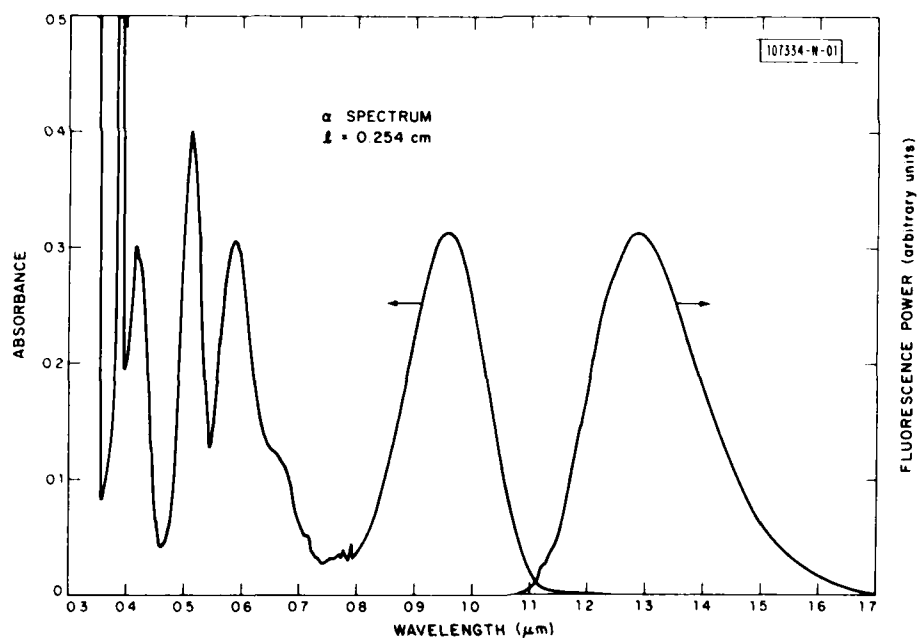
Fig. II-10. α-polarized absorption and fluorescence from V:MnF$_2$ at 77 K.

~0.5 wt% VF_2 and absorbed 45 percent of the incident power. An untuned laser output power at 1.115 μm of up to 120 mW was obtained for 1.9 W of absorbed power. The tuning curve generated at 1.6 W of absorbed power is shown in Fig. II-9. The long-wavelength limit of operation is considerably shorter than would be expected from the fluorescence of $V:MgF_2$; this probably indicates the existence of excited-state absorption from the $^4T_2$ to $^4T_1$ level, which competes with gain from the $^4T_2 \rightarrow {}^4A_2$ transition and reduces the gain to below zero at wavelengths longer than 1.16 μm.

Some spectroscopic properties of $V:MnF_2$ have been examined. The absorption and fluorescence curves for α polarization are shown in Fig. II-10; the $^4T_2 \rightarrow {}^4A_2$ fluorescence lifetime at 77 K was measured to be 3.0 ms. $V:MnF_2$ is interesting for two reasons. One is the possibility of excitation transfer from the Mn^{2+} ions to the V^{2+} ions, which would enhance laser efficiency under conditions of broadband excitation from flashlamps. The other is the shift to longer wavelengths of the $^4A_2 \rightarrow {}^4T_2$ absorption band (compared to $V:MgF_2$) which should allow efficient optical pumping of $V:MnF_2$ by a Nd^{3+} laser at 1.06 to 1.08 μm. (See Sec. III-E for details of the MgF_2 crystal growth.)

<div align="right">P. F. Moulton</div>

C. LINEWIDTH CHARACTERISTICS OF GaAlAs SEMICONDUCTOR DIODE LASERS

Use of semiconductor diode lasers as high-resolution spectral sources requires an understanding of the linewidth characteristics of these devices. Reported here is a study of the power and temperature dependence of the fundamental linewidth of continuously operating GaAlAs single-mode diode lasers. The linewidths were observed to decrease linearly with reciprocal output power with a slope significantly greater than the calculated Schawlow-Townes linewidth at room temperature. At liquid nitrogen temperature, within experimental error, the slope decreased to the Schawlow-Townes limit; there appears a finite contribution to the linewidth in the high-power limit, which is attributed to index fluctuations arising from electron-density fluctuations in the small-gain volume of these devices.

The experiments were carried out on single-frequency channel-substrate-planar (CSP) Hitachi and transverse-junction-stripe (TJS) Mitsubishi diode lasers. The devices were thermally isolated in a dewar to avoid temperature fluctuations, and measurements were carried out as previously described,[7] with the exception that the data-taking and reduction were performed with the assistance of a computer. The Mitsubishi TJS diode lasers usually worked well down to liquid helium temperature in contrast to the Hitachi CSP lasers, which usually operated poorly or not all at 77 K and below. The lineshape remained Lorentzian at all times and was carefully checked by heterodyning against a narrow linewidth and stable external cavity GaAlAs diode laser. Figure II-11 shows such a heterodyne spectrum, which is consistent with similar measurements taken on lead-salt diode lasers by Hinkley and Freed.[8]

The linewidth due to quantum phase fluctuations is given by the modified Schawlow-Townes relation[9]

$$2\Gamma = (h\nu/8\pi P_0)\,(c/nl)^2\,(\ln R - \alpha l)\,(\ln R)\,n_{sp} \tag{II-1}$$

where 2Γ is the full-width at half-maximum of the emission line at frequency ν, P_0 is the single-ended output power, n is the refractive index, l is the cavity length, α is the material absorption coefficient, R is the facet reflectivity, and n_{sp}, the spontaneous emission factor, is
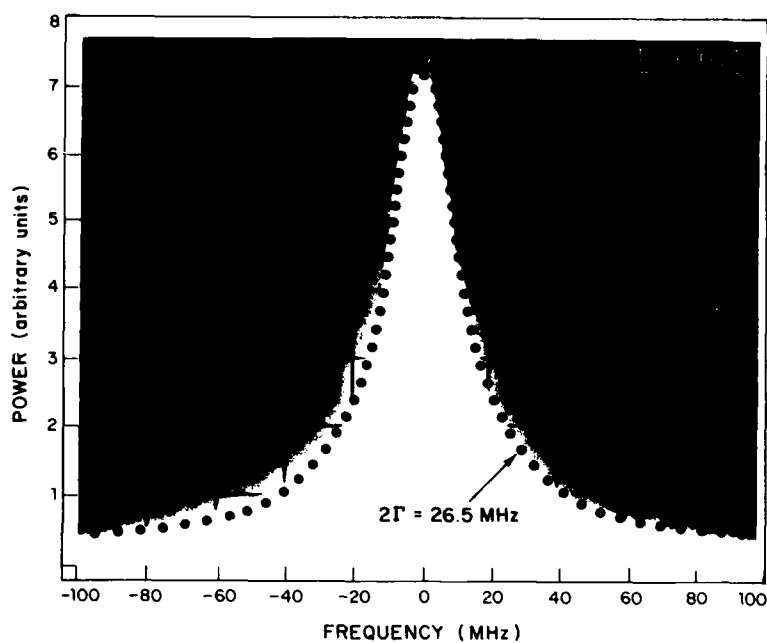
Fig. II-11. Heterodyne spectrum of Hitachi CSP GaAlAs diode laser at room temperature. Output power of 4.2 mW. Dotted curve is a theoretical fit.
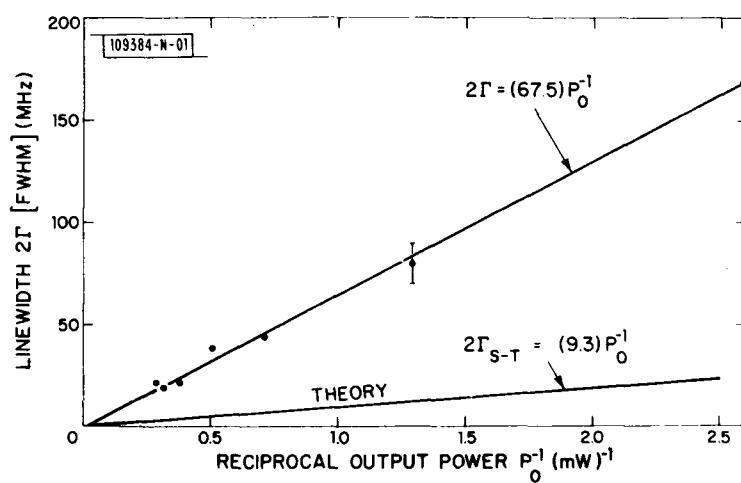
Fig. II-12. Linewidth of Mitsubishi TJS lasers at 273 K compared to calculated Schawlow-Townes width.

the ratio of the spontaneous emission rate per mode to the stimulated emission rate per laser photon. In a semiconductor laser the spontaneous photon emission factor n_{sp} may be written as (Ref. 10)

$$r_{sp} = \{1 - \exp[(h\nu + E_{Fv} - E_{Fc})/kT]\}^{-1} \quad , \tag{II-2}$$

where E_{Fc} and E_{Fv} are the conduction- and valence-band quasi-Fermi levels, k is the Boltzmann constant, and T is the temperature. In most lasers, n_{sp} is nearly unity, but for semiconductor lasers with nondegenerate carrier distribution functions, n_{sp} is greater than unity at room temperature. For these devices, n_{sp} is about 2.3 at room temperature and becomes unity below 77 K.

Figure II-12 shows the linewidth plotted as a function of reciprocal single-ended output power for several Mitsubishi TJS diode lasers at ice temperature together with the calculated linewidth dependence using Eq. (II-1). This discrepancy with theory has been reported[7] previously for the Hitachi CSP diode lasers at room temperature. The difference between the experimental and theoretical slopes is a factor of 7 for the Mitsubishi TJS diodes and a factor of 20 for the Hitachi CSP lasers. This discrepancy between the two types of laser may be due to the difference in their construction. The difference between experimental and theoretical slopes, however, which nearly disappears at low temperature must be explained by some other process.

Fig. II-13. Linewidth vs reciprocal power for Mitsubishi diode lasers at 77 K compared with calculated Schawlow-Townes width.
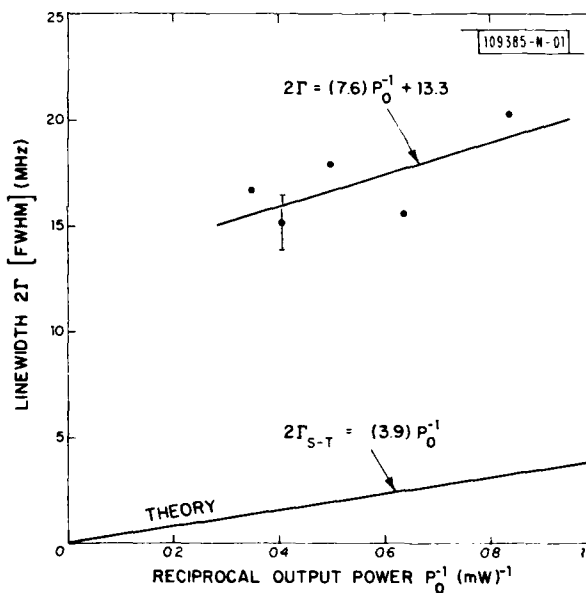
Figure II-13 shows the linewidths measured at 77 K for the Mitsubishi diodes. Within experimental error, the observed slope has a value much closer to that calculated from the Schawlow-Townes expression, but with the unexpected result of a finite intercept of 13 MHz. This finite intercept for $1/P = 0$ occurs at all temperatures, increasing from about 1 to 3 MHz at room temperature to as much as 30 to 40 MHz at liquid helium temperature. This fundamental limit to the laser linewidth is attributed to fluctuations in refractive index in the gain volume of the laser. Such fluctuations are significant for the small-gain volumes in these devices.

The fluctuation in the laser frequency is given by

$$\delta \nu = \frac{\nu \sqrt{N}}{n} \, (\partial n / \partial N) \omega_\ell \qquad\qquad (\text{II}-3)$$

where N is the number of electrons in the gain volume and $(\partial n / \partial N) \omega_\ell$ is the change in refractive index with electron number at the laser frequency. For the Mitsubishi TJS diode lasers at 77 K, $N \simeq 10^7$ electrons, which is estimated from the threshold current, carrier lifetime and a gain volume of $2 \times 0.1 \times 200$ μm. The factor $(\partial n / \partial N) \omega_\ell$ is obtained from the room-temperature value of the change in refractive index with electron density (at a density of 1×10^{18} cm^{-3}, which is approximately the same as our density of 2.5×10^{17} cm^{-3}) as reported by Ito and Kimura.[11] The result is a calculated residual linewidth of about 30 MHz, which is surprisingly close considering the approximations made. The variation of this residual linewidth with temperature is also consistent with the reduced threshold currents.

<div align="right">

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D. ELECTRICAL PROPERTIES OF LASER CHEMICALLY DOPED SILICON

The use of UV-laser-induced chemistry to introduce dopants into semiconductors has recently been described. A pulsed UV laser serves both to release dopant atoms near a semiconductor substrate by photolysis of a gas-phase parent molecule and, simultaneously, to melt the surface of the substrate to allow incorporation of the dopants.[12,13] Previous experiments have examined the application of this doping technique to the formation of ohmic contacts on InP or p-n junctions in Si (Refs. 12,13), but not the electrical properties of the laser-doped material itself. These properties are of importance in evaluating the applicability of laser photochemical doping to other device fabrication problems. Here we report on the electrical properties of UV-laser-doped Si as a function of a number of process parameters. Measurements using two different laser wavelengths, one of which was not absorbed by the gas-phase parent molecules, indicate that processes other than photolysis of gas-phase molecules can be important for doping.

A pulsed UV excimer laser was used to irradiate the Si samples, which were translated normal to the beam axis at rates of 0.25 to 8 mm/min. The single-crystal Si samples had either (100) or (111) orientation and resistivities of 300 to 500 Ω-cm. The amorphous Si films, which were used in investigations of the doping of noncrystalline Si, were produced by chemical vapor deposition (CVD) at 625°C on Si substrates covered with a 2000-Å-thick layer of thermal oxide.

Boron doping of Si using BCl$_3$ gas was examined at two different laser wavelengths. CVD Si samples were irradiated using both 193-nm ArF laser radiation, for which the absorption coefficient of BCl$_3$ was measured to be 0.0019 cm^{-1} Torr^{-1}, and 351-nm XeF laser radiation. At 351 nm, BCl$_3$ had no measurable gas-phase absorption even at pressures of 700 Torr in a 1-cm cell.

Figure II-14 shows the sheet resistance of 5000-Å-thick CVD Si films on SiO$_2$ vs fluence at the substrate for both ArF and XeF laser irradiation. The curves are quite similar, with the lowest sheet resistances obtained with ArF-laser radiation, $\sim$60 $\Omega/\square$, about 1/3 of those obtained with the XeF laser. Figure II-14 also shows sheet resistance vs fluence for B doping of single-crystal, 500-Ω-cm, n-Si using ArF radiation; at fluences above 0.4 J/cm^2 the results

Fig. II-14. Sheet resistance of single-crystal and CVD Si as a function of ArF or XeF laser fluence at the substrate. The sample scan rate is 1 mm/min., the laser pulse rate 2 Hz, and the gas pressure 50 Torr BCl_3.
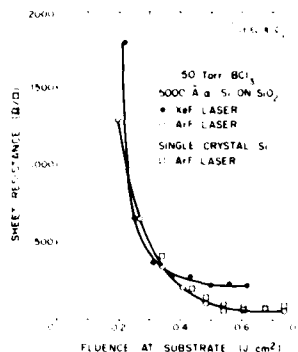
are almost identical to those obtained for CVD Si. The steep rise of the curves at fluences below ~0.2 J/cm^2 is probably due to the threshold for melting of the Si film. In the case of P doping using PCl_3, similar sheet resistance vs fluence curves were obtained for single-crystal substrates.

Table II-1 summarizes the results of Van der Pauw measurements made on single-crystal, amorphous, and polycrystalline Si that was B doped using the ArF laser. Doping profiles of B-doped Si produced under similar conditions have been obtained using secondary ion mass spectrometry;[13] these showed total B doses of 2 to 3 × $10^{15}/cm^2$, in good agreement with the carrier densities obtained here, and doping depths of a few thousand angstroms. Hence, essentially all the B atoms introduced by the UV doping process are electrically activated.

TABLE II-1 ELECTRICAL PROPERTIES OF UV-LASER-DOPED Si. CONDITIONS: 0.7 J/cm^2 AT 193 nm, 50 TORR BCl_3, 1 mm/min. SCAN AT 2 Hz. APPROXIMATELY 35 PULSES PER FOCAL AREA.			
	Sheet Resistance ($\Omega/\square$)	Surface Carrier Density (cm^{-2})	300 K Mobility (cm^2/V-s)
Single-Crystal Si	46	3.3 × 10^{15}	41
5000-Å CVD Si (amorphous)	68	3.7 × 10^{15}	24
5000-Å CVD Si Annealed for 30 min. at 900°C (polycrystalline)	61	2.2 × 10^{15}	47

Somewhat higher mobilities were obtained with single-crystal or polycrystalline (annealed CVD) Si than with amorphous CVD Si. The shallow doping depths imply carrier densities in the 10^{20}-cm^{-3} range, and the low mobility observed in single-crystal Si is due to this high doping density.

In previous studies of laser photodeposition adsorbed films had been shown to play an important role.[14] The role of adsorbed surface layers of BCl_3 in the doping process was investigated by irradiating a sample in an evacuated cell ($P \sim 2 \times 10^{-5}$ Torr). The cell was then filled with 100 Torr BCl_3, re-evacuated, and another portion of the sample irradiated. Figure II-15 shows the results of the measurements; exposure of the sample to BCl_3 prior to irradiation leads to a sheet resistance of 650 $\Omega/\square$ while adding BCl_3 gas to a pressure of 500 Torr reduces the sheet resistance by a factor of ~6.
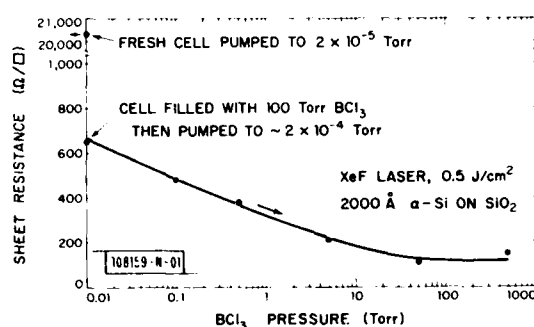
Fig. II-15. Sheet resistance of CVD Si as a function of BCl_3 pressure for a 351-nm fluence of 0.5 J/cm^2. The scan rate is 1 mm/min. and the laser pulse rate is 2 Hz.

The data of Fig. II-15, taken using 351-nm radiation which is not absorbed by BCl_3, provides evidence that adsorbed surface layers can be useful for doping. The 600 $\Omega/\square$ sheet resistance observed for the sample irradiated after exposure to BCl_3 corresponds to a carrier density of 2 to 4×10^{14} cm^{-2}, the uncertainty arising from the possible range of mobilities. The calculated surface density for a monolayer of BCl_3 is 2×10^{14} molecules/cm^2; hence the observed effect is qualitatively consistent with the efficient incorporation of B atoms from the adlayer. These B atoms could be liberated by pyrolysis of the adlayer as the surface is heated, but other processes such as photolysis of the adlayer may also be occurring.

In conclusion, laser chemical doping of Si with B and P has been investigated and shown to involve both gas-phase and surface processes. Dissociation at the surface may occur by photolysis, pyrolysis, or both. Gas-phase dissociation may occur by nonlinear, as well as linear, photochemistry. The mechanisms involved in a particular doping experiment can vary with the doping gas, which may or may not form an adlayer and with laser intensity, which will determine the importance of nonlinear processes. Adsorbed molecular layers can produce significant doping effects.

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E. SUBMILLIMETER SIS MIXERS

Extremely low-noise millimeter-wave detectors and mixers have recently been reported[15] which depend on single-particle tunneling between two superconducting films separated by a thin

oxide layer. The metal-oxide technology for making superconducting-insulating-superconducting (SIS) junctions is highly advanced and can be used to fabricate submicrometer-dimension devices suitable for submillimeter-wave applications.

The combination of excellent low-frequency sensitivities and well-developed fabrication technology make the SIS mixers particularly attractive for systems using antenna structures and arrays at higher millimeter and submillimeter frequencies. The high-frequency limit of SIS devices has never been clearly established experimentally or theoretically. The strong nonlinearity, characteristic of tunneling, indicates that the local oscillator requirements of a heterodyne detector would be very low. Furthermore, the absence of series resistance makes these devices approximate the ideal mixer parameters.[16]

In order to investigate SIS properties in the submillimeter, $Nb-Nb_2O_5-Pb$ diodes were fabricated on quartz with a diameter of 0.7 μm, a junction capacitance of ~ 100 fF, and a normal resistance (R_n) of about 10 Ω. They were immersed in liquid helium and illuminated with focused 693-GHz radiation from an optically pumped formic acid laser. They showed a strong video response to the radiation, which could be differentiated from the regular Josephson effect since it was not affected by a magnetic field.

Harmonic mixing experiments were set up to further probe the detection mechanism at higher frequencies. A V-band klystron, illuminating the SIS device, generated currents at the fifth harmonic which then mixed with carcinotron radiation at 345 GHz. Although there was no antenna structure, IF signal-to-noise ratios of 30 dB were achieved. These results indicate, that by coupling the radiation in more efficiently and by further reducing junction area or by tuning out the junction capacitance with a series inductance, these devices will be useful as high-sensitivity submillimeter detectors and radiometers.

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III. MATERIALS RESEARCH

A. IMPROVED TECHNIQUES FOR GROWTH OF LARGE-AREA SINGLE-CRYSTAL Si SHEETS OVER SiO_2 USING LATERAL EPITAXY BY SEEDED SOLIDIFICATION

Growth of oriented crystalline Si films on insulating layers has been the subject of numerous investigations directed toward the application of silicon-on-insulator structures for high-speed and high-density integrated circuits. Recently, we prepared single-crystal Si films over SiO_2 and Si_3N_4 layers by the technique of lateral epitaxy by seeded solidification (LESS).[1] This report describes several significant improvements in the LESS technique. By using the new procedures, we have prepared continuous single-crystal Si sheets of several square centimeters over SiO_2. N-channel MOSFETs fabricated in these films have electron surface mobilities of 600 to 700 cm^2/V-s, comparable to the values for devices fabricated in bulk Si (Ref. 2).

In the original LESS experiments, a single-crystal Si substrate was first overcoated with an insulating layer. Narrow parallel stripes spaced at 50- or 500-μm intervals were opened to expose the substrate, after which a polycrystalline CVD Si film and CVD SiO_2 cap were deposited over the entire surface. A continuous single-crystal Si film was obtained by using two graphite strip heaters (one of which was movable) for zone melting the Si film. In this process, solidification was initiated within the stripe openings, where it was seeded by the Si substrate, and followed by lateral epitaxial growth over the insulating layer. In most of the experiments, growth proceeded outward in both directions from each stripe opening, so that growth fronts originating from adjacent openings met midway between these openings.

On the basis of our initial LESS results, we suggested[1] that it should be possible to propagate a single-crystal Si film indefinitely from a single stripe opening by the controlled motion of a narrow molten zone formed parallel to the opening, although the maximum distance of single-crystal overgrowth that had been achieved was only about 4 mm. The growth was limited primarily because the motion of the upper strip heater, which was manually adjusted, was not controlled well enough to produce uniform zone melting of the Si film over the entire stripe opening. Moreover, during zone melting the Si film had a tendency to agglomerate (bead up) in regions outside the stripe openings, frequently causing lateral overgrowth to be interrupted. In the present investigation we have overcome these difficulties by using a motor-driven upper strip heater to achieve controlled motion of the molten Si zone and by using a dual-dielectric encapsulation layer to enhance the stability of the Si film during zone melting. In addition, two improved versions of the original seeding procedure have been developed.

As in the original LESS experiments, two graphite strip heaters were used in this investigation: a stationary sheet, on which the sample is placed with the Si film face up, and a narrow movable bar positioned about 1 mm above the sample. Figure III-1 shows schematically the heater configuration and the two different seeding procedures used. The first procedure employs the sample structure shown in Fig. III-1(a). Seeding is accomplished by means of a single stripe opening in a recessed SiO_2 growth mask prepared by thermal oxidation of a $\langle 100 \rangle$Si substrate. A planar surface is formed by the SiO_2 mask and the Si substrate exposed by the stripe opening. A CVD poly-Si film 0.5 μm thick is then deposited over the entire surface, and the sample is capped sequentially with a 2-μm film of CVD SiO_2 and a 300-$\mathring{A}$ film of sputtered Si_3N_4. The use of such a dual-dielectric (Si_3N_4/SiO_2) encapsulating layer has been found to greatly enhance the extent of single-crystal growth produced by LESS processing. This layer prevents the

(a)

MOVABLE UPPER STRIP HEATER

LOWER STRIP HEATER

108100#-02

Si $\langle 100 \rangle$ SUBSTRATE

300 Å Si_3N_4/2 μm SiO_2 CAP
0.5 μm CVD POLY-Si FILM
0.5 μm RECESSED SiO_2 MASK

(b)

EXTERNAL SEED

Si_3N_4/SiO_2
POLY-Si
SiO_2
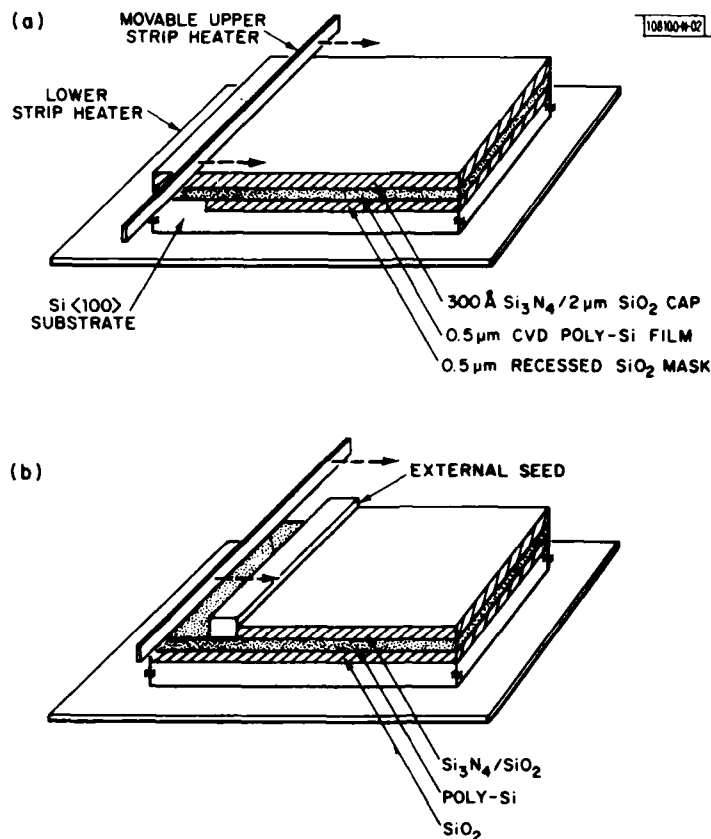
Fig. III-1. Schematic diagram showing the two different seeding procedures used in the LESS process for growth of large-area single-crystal Si sheets over SiO_2.

Si film from agglomerating as the molten zone propagates laterally[3] and also prevents contamination of the film during the high-temperature treatment.

The sample structure for the second seeding procedure, which employs an external Si seed, is shown in Fig. III-1(b). This structure is similar to the one shown in Fig. III-1(a), except that the $\langle 100 \rangle$ Si substrate is completely masked with thermal SiO_2 before deposition of the poly-Si film, the Si_3N_4/SiO_2 cap is etched away along one edge of the sample to expose the poly-Si film, and a narrow strip (about $2 \times 0.2 \times 0.03$ cm) cut from a $\langle 100 \rangle$ single-crystal wafer is placed on the exposed surface of the poly-Si film to serve as an external seed. Thus the lateral growth is seeded from the top in the second procedure and from the bottom in the first procedure. For both procedures the sample size was typically about 2.5×2.5 cm.

The LESS experiments were performed in a flowing Ar ambient. In each run the stationary graphite sheet was heated to ~1300°C in about 10 s. The upper graphite strip, which has its long axis parallel to the long direction of the stripe opening or external seed, was heated sufficiently to melt a narrow zone in the Si film adjacent to the seed. The strip was then scanned across the sample at a speed of 0.1 to 0.2 cm/s, causing the molten zone to traverse the sample. The entire Si film was recrystallized by a single scan.

After LESS processing, the samples were routinely examined by optical microscopy in the interference contrast mode. The zone-melted Si films prepared by both procedures have mirror-smooth surfaces indistinguishable from those of the as-prepared poly-Si films. Such smooth surfaces were not obtained for the Si films recrystallized in those earlier LESS experiments where growth fronts originating from adjacent stripe openings met midway between the openings. Those films had distinct surface features located along the line of intersection between the growth fronts.

X-ray and reflection high-energy electron diffraction analysis shows that the recrystallized Si films have the same crystallographic orientation as the seed over areas as large as 2×2 cm. TEM analysis indicates that the films have very few crystallographic defects such as dislocations, stacking faults, and twins. The use of a recessed SiO_2 layer adjacent to the stripe opening [Fig. III-1(a)] seems to reduce twin formation. Figure III-2 shows a bright-field TEM micrograph and an electron diffraction pattern for a Si film produced in the present experiment. Strong

108099-R-01

10 μm

(a)

Fig. III-2. Bright-field TEM micrograph (top) and electron diffraction pattern (bottom) for a single-crystal Si film grown over SiO_2 by the LESS technique.

(b)
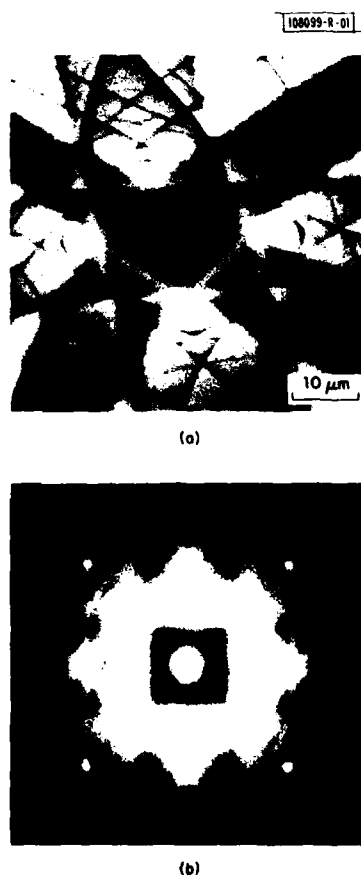
(100) bend contours are observed throughout the entire Si film. In some locations these contours exhibit slight discontinuities indicating the presence of linear features of unknown origin. The sharp Kikuchi lines and bands in the electron diffraction pattern indicate the film is of high crystalline quality.

There does not appear to be any fundamental limit on the distance of single-crystal Si growth that can be achieved by lateral solidification seeded by either of the new procedures. At present, the extent of single-crystal overgrowth is limited by the dimensions of the strip-heater system. There should be no difficulty in scaling up the system for processing full-size wafers. In addition, the use of an external seed should permit the use of substrates other than single-crystal Si, such as fused silica.

As an initial demonstration of the device potential of the single-crystal Si films produced by the LESS technique, we have fabricated n-channel, polysilicon gate MOSFETs on these films. For comparison, similar devices were fabricated on commercial silicon-on-sapphire (SOS) wafers (with 0.5-μm-thick Si) in a parallel run. The transistors have a gate width of 25 μm and gate lengths of 6, 12, or 25 μm. Figure III-3 shows typical I-V characteristics of devices with a 6-μm gate length fabricated on a LESS single-crystal Si film [Fig. III-3(a)] and on SOS [Fig. III-3(b)]. For the LESS devices the electron surface mobilities determined from the linear region of the I-V curves are in the range of 600 to 700 cm^2/V-s, comparable to the values for devices fabricated on bulk Si (Ref. 3). In comparison, the SOS devices have electron mobilities of 350 to 400 cm^2/V-s.

(a)

(b)
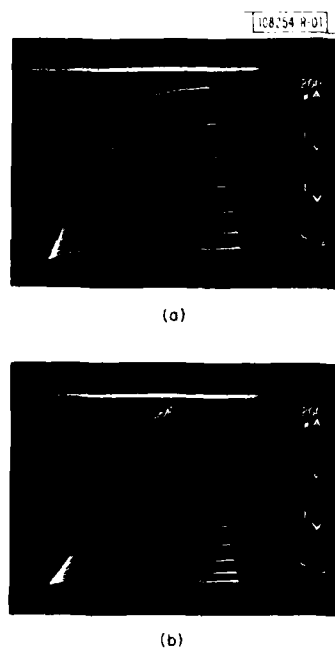
Fig. III-3. Source-drain I-V characteristics (V_G = 0 to 6 V) of MOSFETs fabricated on (a) a LESS Si film, (b) SOS. The devices have a gate width of 25 μm, gate length of 6 μm, and gate oxide thickness of 1000 Å.

On the basis of the excellent characteristics of the MOSFETs fabricated on the LESS Si films, we believe that silicon-on-insulator structures prepared by the LESS technique show great promise for the fabrication of high-performance integrated circuits.

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B. EFFICIENT Si SOLAR CELLS BY LOW-TEMPERATURE SOLID-PHASE EPITAXY

Conventional techniques for junction formation in Si solar-cell processing utilize either high-temperature diffusion or ion implantation followed by thermal annealing. The diffusion or annealing treatments, which are usually carried out at 850° to 1000°C for extended periods, frequently result in degradation of substrate materials. Moreover, in the fabrication of low-cost solar cells on polycrystalline materials, such high-temperature treatments can have adverse effects either because of rapid dopant diffusion along the grain boundaries, which may cause shorting of the junction, or because of generation of electrically active defects.

This report describes a low-temperature technique that uses solid-phase epitaxy (SPE) to produce p-n junctions for Si solar cells. In annealing experiments at 400° to 500°C on samples prepared by depositing a thin Al film and then an amorphous-Si (a-Si) film on $\langle 100 \rangle$ Si substrates, it was found that a single-crystal SPE Si layer is formed by transport of Si atoms from the a-Si film through the Al film to the surface of the substrate;[4] the SPE layer is strongly p-type due to Al doping.[5] We have utilized this simultaneous crystal growth and doping process to produce p-n junctions on n-type Si substrates. Solar cells with conversion efficiencies at AM1 up to 10.4 and 8.5 percent have been fabricated on $\langle 100 \rangle$ single-crystal and polycrystalline substrates, respectively, without using an antireflection (AR) coating or back-surface field.

Thin films of Al and a-Si, each 0.2 μm thick, were deposited sequentially by e-beam evaporation on 1-Ω-cm n-type $\langle 100 \rangle$ Si or Wacker polycrystalline Si substrates. The polycrystalline substrates, which had a grain size of 0.5 to 3 mm, were etch-polished with a $5HNO_3:3HF:3CH_3COOH$ solution. The $\langle 100 \rangle$ Si wafers were 300 μm thick, while the etched polycrystalline substrates were 250 μm thick. Both types of substrates were chemically cleaned by conventional procedures, and immediately before loading into the vacuum evaporation system they were etched in dilute HF to remove native oxides. After deposition the samples were annealed at 400° to 500°C for 0.5 to 15 hr in a tube furnace with flowing N_2 ambient. These temperatures are far below the Si-Al eutectic temperature of 577°C.

Solid-phase transport of Si atoms from the amorphous film through the Al film occurs rapidly during annealing. The driving force for transport and SPE growth is provided by the excess free energy of the metastable a-Si relative to the stable crystalline phase.[4] For $\langle 100 \rangle$ substrates, formation of the SPE Si layer reaches completion after 4 hr at 400°C or 30 min. at 500°C. Figure III-4 shows Auger depth profiles for a sample before [Fig. III-4(a)] and after [Fig. III-4(b)] annealing at 500°C for 30 min. After annealing, the Al film is confined to the outer surface, and the interface between this film and the SPE Si layer is quite sharp. The epitaxial character of the grown layers was confirmed by x-ray diffraction and [4]He[+] ion backscattering measurements. Figure III-5 shows the random and $\langle 100 \rangle$-aligned backscattering spectra for such a layer measured after the Al film on the surface had been removed by etching. The minimum backscattering yield is about 6 percent near the surface, compared to 4 percent for a virgin $\langle 100 \rangle$ Si crystal. For films on polycrystalline substrates, epitaxial growth occurred within each individual grain. Longer annealing times were required for completing the process because other crystal orientations have slower SPE rates than the (100) plane.[6]

For $\langle 100 \rangle$ samples annealed at 500°C, the Al films were etched off and room-temperature Hall measurements were made on the SPE Si layers. The as-grown layers are p-type with a hole concentration of 2×10^{18} cm^{-3} and Hall mobilities of ~70 cm^2/V-s. Additional annealing
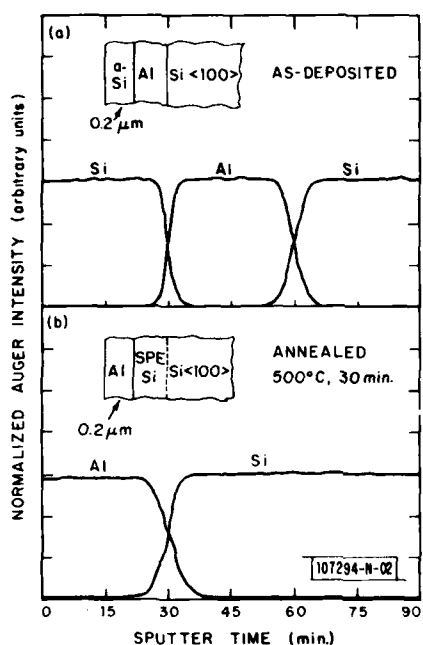
Fig. III-4. Auger depth profiles
for a-Si/Al/⟨100⟩Si sample (a)
before and (b) after annealing at
500°C for 30 min.
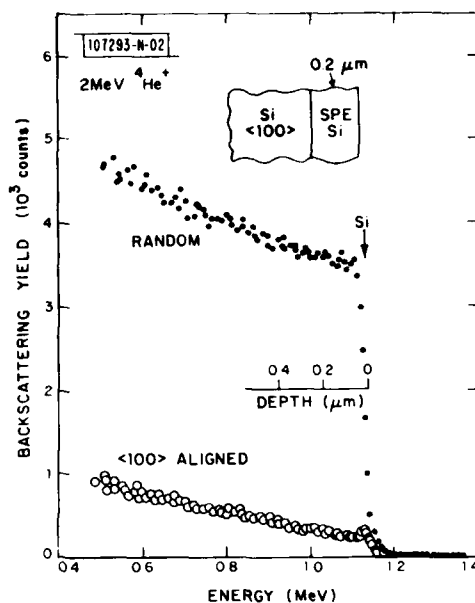
Fig. III-5. Random and ⟨100⟩-aligned
ion backscattering spectra for SPE Si
film grown on a ⟨100⟩Si substrate.
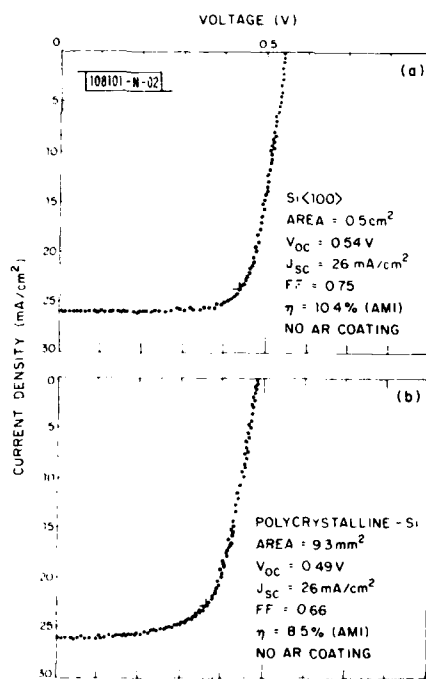
Fig. III-6. Photocurrent density as
a function of voltage for solar cells
with SPE junctions fabricated on
(a) ⟨100⟩Si and (b) polycrystalline-
Si substrates.
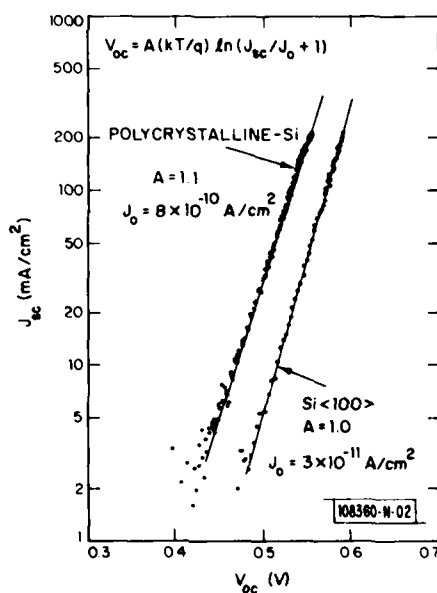
Fig. III-7. Short-circuit current
density J_{SC} as a function of open-
circuit voltage V_{OC} at different
illumination levels for the cells
of Fig. III-6.

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at 900°C for 30 min. yields a hole concentration of 2×10^{19} cm^{-3} and Hall mobility of ~25 cm^2/V-s. The measured hole concentrations are in agreement with the reported solid solubilities of Al in Si at 500° and 900°C (Ref. 7). These results suggest that there was additional Al in the nonsubstitutional sites at 500°C which becomes substitutional during the 900°C anneal. The relatively high channeling yield (~6 percent) observed in the SPE layers may be partially caused by dechanneling from nonsubstitutional Al. The p-n junction depths determined by grooving and staining are 0.20 to 0.23 μm, equal within experimental error to the thickness of the initial a-Si film. (A few experiments were performed with a-Si films ~0.1 μm thick. The junction depth was again equal to the film thickness.)

More than 20 solar cells, with areas of about 0.3 × 0.3 or 0.5 × 1.0 cm^2, have been fabricated from the annealed samples. In some cases the front contact was made by patterning the as-grown Al film, which makes good ohmic contact to the SPE p-Si layer. Usually, however, the Al film was removed by etching, and vacuum-evaporated Au or Al was used for the front contact. The cells were not AR coated. All the cells have very similar operating characteristics. Figure III-6 shows typical current-voltage curves taken under simulated AM1, one-sun illumination for a single-crystal cell [curve (a)] and a polycrystalline cell [curve (b)]. The former cell has an open-circuit voltage V_{oc} of 0.54 V, short-circuit current density J_{sc} of 26 mA/cm^2, and fill factor FF of 0.75, for a measured efficiency η of 10.4 percent. The corresponding V_{oc}, J_{sc}, FF, and η values for the polycrystalline cell are 0.49 V, 26 mA/cm^2, 0.66 and 8.5 percent. Use of an AR coating would be expected to improve the efficiencies to 14 percent for the single-crystal cell and 11 to 12 percent for the polycrystalline cell. Figure III-7 shows the dependence of J_{sc} on V_{oc} for the two cells of Fig. III-6 as obtained by a series of measurements at different illumination levels up to about 10 suns. From the relationship $V_{oc} = A(kT/q) \ln(J_{sc}/J_0 + 1)$, where k is Boltzmann's constant, T the absolute temperature and q the electron charge, one obtains a diode factor A of 1.0 and saturation current density J_0 of 3×10^{-11} A/cm^2 for the single-crystal cell and A = 1.1 and $J_0 = 8 \times 10^{-10}$ A/cm^2 for the polycrystalline cell. The near unity values of A indicate that current collection in the cells is dominated by diffusion, implying that the junctions are abrupt and of good quality. The increases in A and J_0 for the polycrystalline cell are probably due to junction leakage caused by conduction through grain boundaries or defects within the grains.

Significant improvement in solar cell performance can be expected by optimizing the substrate carrier concentration and the junction depth (which is conveniently adjusted by varying the thickness of the a-Si film), as well as by using a back-surface field and AR coating. If donor dopants (Sb, for example) can be used as transport media for low-temperature SPE of Si, this technique can also be employed for the formation of p-n junctions for n/p solar cells and for obtaining back-surface fields for p/n cells. As a low-temperature method that yields both a p-n junction and a low-resistance metal contact, the SPE technique should be highly advantageous for Si solar-cell fabrication, particularly on polycrystalline substrates.

B-Y. Tsaur   J. C. C. Fan
G. W. Turner   C. H. Anderson

C. ORIENTATION DEPENDENCE OF VERTICAL GROWTH RATES IN VAPOR-PHASE EPITAXY OF InP

Preparation of single-crystal sheets of InP over dielectric films by means of lateral growth using the PCl$_3$-InP-H$_2$ method of vapor-phase epitaxy was reported previously.[8] To obtain such

a sheet, a single-crystal InP substrate is coated with a phosphosilicate glass (PSG) film, patterned openings are etched in the film, and growth conditions are fixed so that nucleation occurs only on the areas of the substrate exposed by the openings. When the thickness of the InP epilayers grown vertically on these areas exceeds the thickness of the PSG, these layers can seed lateral growth over the PSG. The effectiveness of this growth procedure in forming InP sheets increases as the ratio of the lateral to vertical growth rates increases. To obtain satisfactory results, substrates with low-index orientations are used, since these have the lowest vertical growth rates.

As part of our previous study,[8] we made preliminary measurements of the relative vertical growth rates on the principal low-index planes – (111)A, (111)B, (100), and (110). We have now used similar methods of measurement to evaluate growth rates on these planes as a function of substrate temperature. In order to obtain reliable rate data it was necessary to take account of systematic changes in the deposition of InP that we have found to occur in any series of growth runs made with the same InP source ingot, even under fixed experimental conditions. In the first two or three runs with a fresh source, the deposit usually consists of clumps of discrete crystallites that are not epitaxial. In later runs the deposit is epitaxial, but the growth rate generally decreases from run to run. Our vertical growth rate measurements were therefore
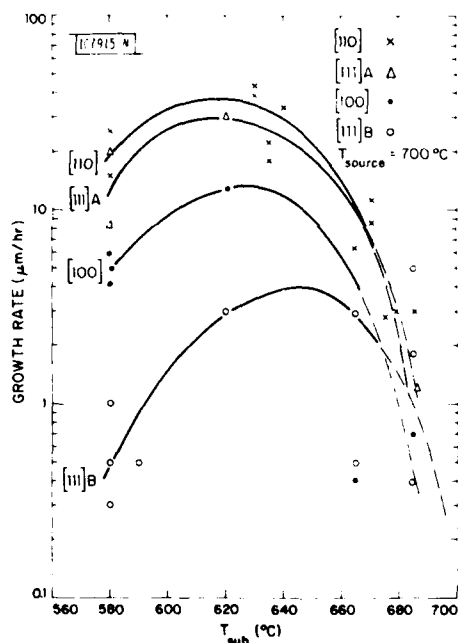
Fig. III-8. Growth rates of InP on (111)B, (111)A, (100), and (110) InP substrates vs substrate temperature for a source temperature of 700 C.

made in the first few runs in which epitaxial growth was obtained with each new source. Figure III-8 shows the rates measured as a function of substrate temperature between 580° and 690°C in experiments where the control temperature for the InP source was 700°C and the mole fraction PCl_3 in the gas stream entering the source zone was 2×10^{-3}.

All the (111)A and (100) growth rate data plotted in Fig. III-8 were obtained from runs in which (111)B data were also measured. In such runs the (111)A and (111)B rates were found

by measuring the thickness of epilayers grown on the opposite sides of the same (111) substrate, while the (100) and (111)B rates were measured for epilayers grown on (100) and (111) substrates placed side by side in the reactor. The (110) growth rate data plotted in Fig. III-8 were obtained from runs in which thickness measurements were made on epilayers grown on the (110) and (100) surfaces of the same substrate. To find the (110) growth rate, the ratio of (110) to (100) thickness was multiplied by the rate read off the (100) curve in Fig. III-8 for the same substrate temperature.

All four curves plotted in Fig. III-8 exhibit the same qualitative variation of growth rate with substrate temperature. Over most of the temperature range, however, the (111)B rate is much lower than the values for the other three orientations, indicating that growth is kinetically controlled. At 580°C, for example, the re. ˙i.˙ rates are 1, 10, 27, and 40 for (111)B, (100), (111)A, and (110), respectively.

For orientations other than (111)B, epitaxial growth completely covering the substrate surface was observed at temperatures even below 580°C. In the case of (111)B surfaces no epitaxial growth took place at these temperatures, although rapid non-epitaxial deposition did occur. When the substrate temperature was increased above ~580°C, epitaxial growth took place on some regions of the (111)B surface, with non-epitaxial deposition still occurring on the remainder. As the temperature was further increased, the extent of epitaxial growth also increased, and at temperatures above ~620°C this growth covered the entire surface. The epitaxial regions had a terraced surface morphology, with some randomly distributed hillocks also present. The growth rates plotted in Fig. III-8 were measured for hillock-free areas. For the (111)B orientation, these rates were below 1 μm/hr at the lowest temperature that yielded epitaxial growth. With increasing temperature the (111)B growth rate increased to a maximum of 3 to 4 μm/hr in the vicinity of 650°C, then decreased rapidly. Observations made in lateral growth experiments indicate that the vertical growth rates for the other three orientations reach their maxima at temperatures somewhat below 650°C. It appears that at the highest temperatures these rates decreased so rapidly that they became lower than the (111)B rate, since in experiments at these temperatures continuous epitaxial layers were obtained on (111)B surfaces while some regions of surfaces with other orientations exhibited thermal decomposition. Accordingly, at the high temperature end of the plot in Fig. III-8 the curves for the other orientations cross the (111)B curv , although in this region the curves are dashed because the reliability of the data is significantly reduced by the increasing effects of thermal decomposition and etching by HCl vapor.

<div align="right">P. Vohl</div>

D. THEORETICAL MODEL FOR PULSED ENERGY-BEAM CRYSTALLIZATION OF AMORPHOUS SEMICONDUCTOR FILMS

We previously presented a theoretical model describing scanned CW laser crystallization of a thin amorphous semiconductor film on a thick substrate.[9] This model, which takes account of the latent heat emitted in the irreversible transformation from the amorphous to the crystalline state, has now been extended to the case of pulsed energy-beam crystallization. We have obtained numerical solutions of a nonlinear integral equation describing the radial motion of the amorphous-crystalline (a-c) phase boundary in a thin film in response to a heat pulse. These solutions yield three types of motion – a series of jumps, a single longer jump, or indefinite runaway – that account for the structural features observed in pulsed laser and electron-beam crystallization.

Our model assumes a Gaussian heat pulse of cylindrical symmetry incident on an amorphous semiconductor film at $t = 0$. Although the film is supported on a substrate, we reduce the problem to a two-dimensional one by assuming that a fraction f of the incident pulse energy is deposited in the film and that the heat pulse decay into the substrate is described by an exponential damping factor $\exp[-\gamma t]$. The temperature distribution in the film due to the heat pulse alone is given as a function of time by the expression

$$T_P(r, t) = \frac{fQ \exp[-\gamma t]}{\rho C} \left\{ \frac{\exp[-r^2/4\kappa(t + t_o)]}{4\pi\kappa(t + t_o)} \right\} \tag{III-1}$$

where fQ is the heat input of the pulse per unit film thickness, ρ is the density of the film, C its specific heat, and κ its effective diffusivity. The term in braces describes the time evolution of a heat pulse[10] that is a Gaussian of width $r_o \equiv [4\kappa t_o]^{1/2}$ at $t = 0$.

The temperature distribution in the film also has a contribution due to the latent heat emitted as the a-c boundary moves forward. This contribution is given by an integral over the heat emitted at earlier times of the form[11]

$$T_L(r, t) = \frac{fL}{2C\kappa} \int_0^t \frac{R(t') \dot{R}(t')}{(t - t')} \exp[-\gamma(t - t')]$$

$$\times \exp\left\{-[r^2 + R^2(t')]/4\kappa(t - t')\right\} I_0\left[\frac{rR(t')}{2\kappa(t - t')}\right] dt' \tag{III-2}$$

where L is the latent heat of transformation, $I_0(x)$ is a Bessel function of the second kind, $R(t')$ is the position of the a-c boundary at time t', and $\dot{R}(t')$ is its velocity.

The total temperature distribution can be written

$$T(r, t) = T_P(r, t) + T_L(r, t) + T_b \quad , \tag{III-3}$$

where T_b is taken to be a uniform background temperature. If we now assume that the a-c transformation occurs when the boundary reaches a critical temperature T_c (Ref. 9), then the motion of the boundary is described by the integral equation

$$T_c = T_P[R(t), t] + T_L[R(t), t] + T_b \quad . \tag{III-4}$$

Since the a-c transformation is irreversible we add the physically necessary condition that if the radial velocity of the a-c boundary approaches a negative value, the boundary comes to rest and its temperature begins to drop below T_c. The a-c boundary then remains at rest until such time as the diffusing heat pulse raises its temperature to T_c, and it begins to move again. For convenience in computation, Eq. (III-4) can be written in terms of normalized quantities as

$$1 = \frac{\beta \exp[-\Gamma\tau] \exp[-u^2(\tau)/(1 + \tau)]}{(1 + \tau)} + \xi \int_0^\tau \frac{u(\tau') \dot{u}(\tau')}{(\tau - \tau')} \exp[-\Gamma(\tau - \tau')]$$

$$\times \exp\left\{-[u^2(\tau) + u^2(\tau')]/(\tau - \tau')\right\} I_0\left[\frac{2u(\tau) u(\tau')}{(\tau - \tau')}\right] d\tau' \quad , \tag{III-5}$$

where

$$\beta = \frac{fQ}{\pi r_o^2 (T_c - T_b) \rho C} \quad , \quad \xi = \frac{2fL}{C(T_c - T_b)} \quad , \quad u = R/r_o \quad ,$$

$$\dot{u}(\tau) = \frac{du(\tau)}{d\tau} \quad , \quad \tau = t\frac{4\kappa}{r_o^2} \quad , \quad \Gamma = \frac{\gamma r_o^2}{4\kappa} \quad .$$

In the absence of the latent heat term, Eq. (III-5) determines the values of the normalized radius $u(\tau)$ as a function of τ for which the temperature due to the heat pulse alone is T_c. We will refer to the curve of $u(\tau)$ vs τ for this case as the $T'_p = 1$ isotherm. The a-c boundary will always extend beyond this isotherm because of the latent heat contribution.

Fig. III-9. Plot of $u(\tau)$ vs τ for energy-beam crystallization for $\Gamma = 0.1$, $\beta = 3.6$, and $\xi = 0.22$, 0.255, and 3.0. The dashed line represents the $T'_p = 1$ isotherm for $\Gamma = 0.1$ and $\beta = 3.6$. See text for definitions of symbols.
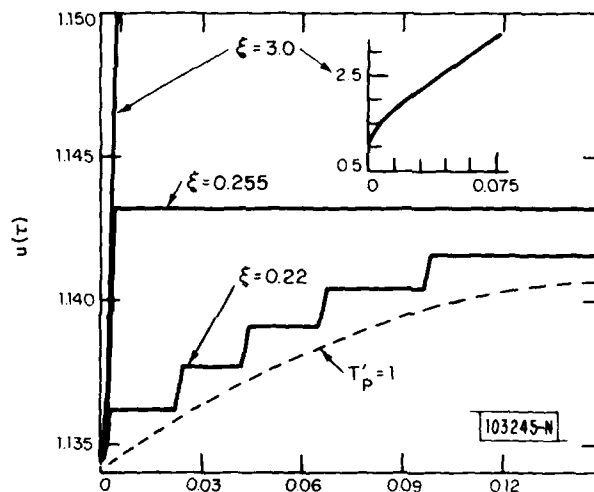
We have solved Eq. (III-5) numerically with the following conditions: at $\tau = 0$, $\dot{u}(\tau) = 0$; $u(0)$ is given by $1 = \beta \exp[-u^2(0)]$; $\dot{u}(\tau) = 0$ if the numerical solution yields $\dot{u}(\tau) < 0$. Because of computational difficulties in solving nonlinear integral equations with singularities in the integrand, the numerical solutions are not reliable quantitatively, but a number of checks indicate that those solutions are qualitatively correct. The results are most sensitive to the latent heat parameter ξ, which increases rapidly as T_b increases toward T_c. The types of a-c boundary motion that can be obtained are exemplified in Fig. III-9, which shows plots of $u(\tau)$ vs τ for three values of ξ, with $\beta = 3.6$ and $\Gamma = 0.1$.

For $\xi = 0.22$, the boundary initially jumps forward a small distance, stopping when the boundary temperature drops below T_c because the drop in T_p can no longer be compensated by the contribution of T_L. As the heat pulse spreads, the temperature at the new position of the boundary eventually reaches T_c, and the boundary again jumps forward. The dashed line in Fig. III-9 represents the position of the $T'_p = 1$ isotherm for this case. It can be seen that the onset of a-c boundary motion occurs at points just ahead of this isotherm, as might be expected. The series of jumps continues until the diffusing heat pulse can no longer raise the temperature of the a-c boundary to T_c, and the boundary comes to rest permanently. The variations in crystallization velocity associated with such intermittent motion of the boundary can account for the structure of concentric rings appearing in amorphous films of Si crystallized by an electron beam.[12]

Fig. III-10. Schematic diagram of system for growth of transition-metal-doped MgF$_2$ crystals by vertical gradient-freeze technique using self-sealing graphite crucibles.

Fig. III-11. Vertical temperature profiles in smaller (left side) and larger (right side) systems used for growth of transition-metal-doped MgF$_2$ crystals. The vertical line in each plot indicates the position of the tungsten mesh heating element.
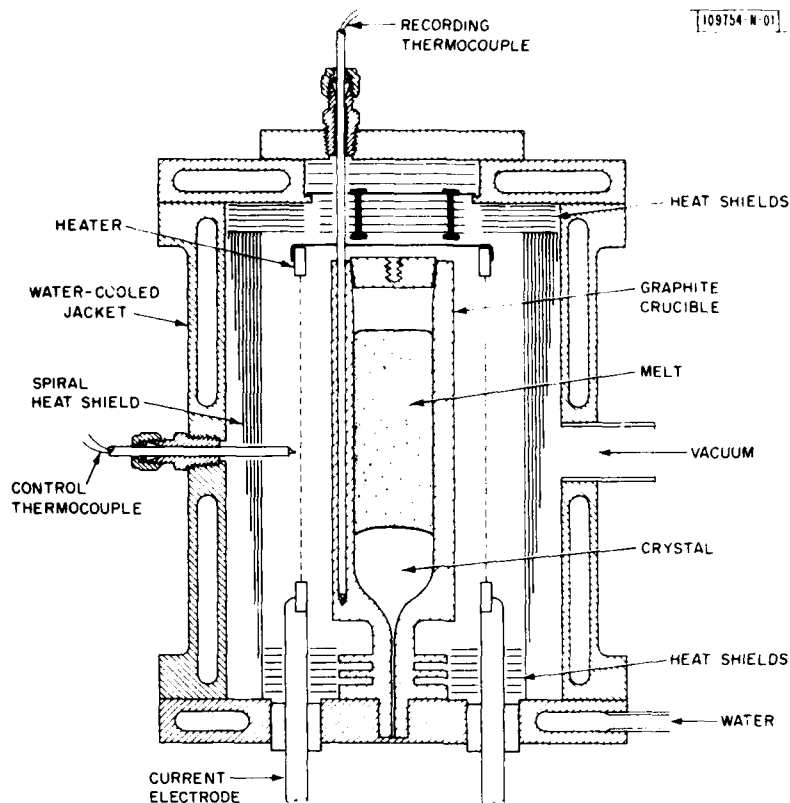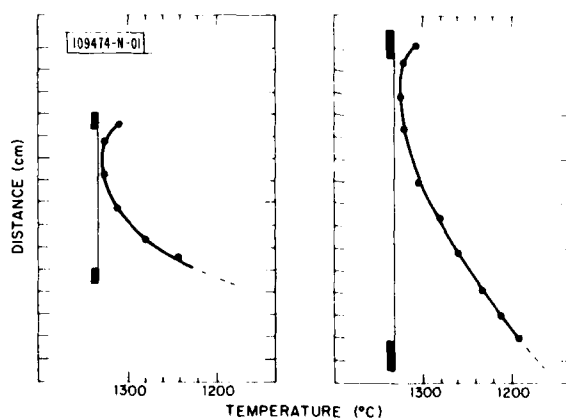
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For $\xi = 0.255$, corresponding to an increase in fl. or T_b, the boundary initially jumps forward by a considerably greater distance than for $\xi = 0.22$. However, the new position of the boundary is so far beyond the $T'_p = 1$ isotherm that the diffusing heat pulse can never raise the temperature to T_c at the boundary, which therefore remains fixed after only one jump. This result is consistent with micrographs of an ion-implanted, ruby-laser-annealed Si surface shown in Ref. 13.

For sufficiently large $u(\tau)$, it can be shown analytically that Eq. (III-5) has a solution with constant normalized radial velocity given by

$$u = \left[\frac{4\Gamma}{\xi^2 - 4} \right]^{1/2} .$$

Thus, "runaway" will occur for $\xi > 2$. In this case, as illustrated by the curves for $\xi = 3.0$ shown in Fig. III-9, the moving a-c boundary can provide sufficient heat to maintain its motion indefinitely. We believe that this corresponds to the case of "explosive" crystallization observed in a number of experiments.[14]

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E. GROWTH OF LASER-QUALITY MgF$_2$ CRYSTALS DOPED WITH Ni, Co, OR V

Several years ago we reported the growth of Ni:MgF$_2$ single crystals by a vertical gradient-freeze technique that uses self-sealing graphite crucibles to prevent loss of the transition-metal fluoride by vaporization.[15] This report describes two recent developments of this technique: increasing the crystal size from about 60 g to about 300 g and doping with Co^{2+} and V^{2+} as well as Ni^{2+}. These developments have been motivated by two potential applications: the utilization of all three transition-metal-doped materials for tunable lasers in the 1- to 2-μm wavelength region and the employment of V:MgF$_2$ as an active medium for laser-fusion drivers. Laser rods exhibiting CW operation at 77 K have been fabricated from crystals grown from charges containing 0.5 to 1.5 wt% of NiF$_2$, CoF$_2$ or VF$_2$.

The system being used for gradient-freeze growth of the larger crystals is shown schematically in Fig. III-10. The growth furnace is heated by means of a cylindrical tungsten mesh resistance element that is enclosed in a water-cooled, stainless-steel jacket, permitting either vacuum or inert-gas operation. The inside diameter of the jacket is 15 cm, compared with 11 cm in the system used for growing smaller crystals. Multilayer molybdenum heat shields are used for thermally insulating the element and the graphite crucible, which is cooled from the bottom by contact with the water-cooled base of the furnace. A charge consisting of MgF$_2$ and the desired quantity of transition-metal difluoride is placed in the crucible, which is tapered near the bottom, ending in an open capillary about 1 mm in diameter and 5 cm long. For seeded growth, the top of the capillary is enlarged to permit insertion of an oriented seed with round or square cross section. The crucible is closed at the top with a tapered graphite plug and then mounted in the furnace. The diagram shows the location of the growth interface at a time part way through a crystal growth run.

The vertical heat shield is a spiral which is wound so that the number of molybdenum layers decreases continuously from ten at the top to two at the bottom. Figure III-11 shows typical vertical temperature profiles generated by this spiral shield design for the larger and smaller
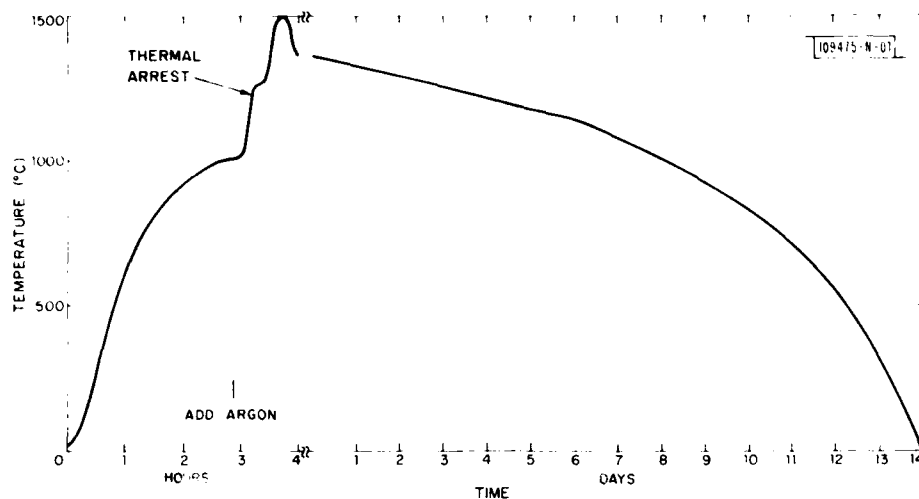
Fig. III-12. Typical time-temperature plot for unseeded growth of transition-metal-doped MgF_2 crystals.
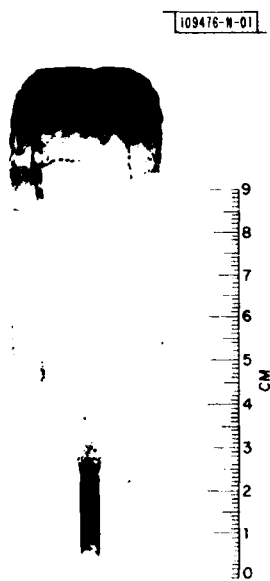

Fig. III-13. Single crystal of Co:MgF_2 grown from a seed with its long axis perpendicular to the c-axis.

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growth systems. In the larger system the temperature gradient along the crucible has been reduced by increasing the number of heat shields above and below the crucible.

Figure III-12 is a plot of temperature vs time for a typical crystal growth run. With the furnace chamber evacuated, the crucible is heated to about $1000\,^\circ C$. The chamber is back-filled with Ar at atmospheric pressure, and heating is continued. For unseeded growth the crucible temperature monitored near the top of the tapered section is increased to about $1500\,^\circ C$ to insure dissolution of the transition-metal fluoride. When the charge begins to melt, as indicated by the occurrence of a thermal arrest, liquid MgF_2 runs down into the capillary, where it freezes to form a polycrystalline plug that seals the capillary. Since the crucible rests on the water-cooled furnace base, the plug remains solid even at the highest temperature. The temperature is rapidly decreased to about $1375\,^\circ C$ ($100\,^\circ C$ above the melting point of MgF_2), then decreased at 2.5 to $5\,^\circ C/hr$ so that the molten charge is gradually solidified from the bottom up. During slow cooling the crystal becomes single before the solid-melt interface reaches the top of the capillary. The same procedure is used for seeded growth, except that the monitored temperature is raised to only $1375\,^\circ C$ so that the seed is not completely melted. After the charge is solidified, the furnace is cooled to room temperature over a period of 3 or more days. The entire cooling cycle is programmed by means of a microprocessor.

Crystals of $Ni:MgF_2$, $Co:MgF_2$, and $V:MgF_2$ up to 3.7 cm in diameter and 10 cm long have been grown by the self-sealing crucible technique. Almost all the crystals grown to date have been unseeded. The long axis of most of the unseeded crystals is at an angle of about $30\,^\circ$ to the c-axis. For crystals doped with Ni^{2+} or Co^{2+} ions, the intensity of the color due to absorption by these ions is quite uniform. However, for most of the crystals doped with V^{2+} ions the intensity decreases somewhat toward the last-to-freeze end.

An x-ray fluorescence technique that we have developed was used to analyze the first-to-freeze region of a number of crystals grown from charges containing up to 1 wt% VF_2. The ratio of the VF_2 content in this region to that in the charge ranges from 1.06 to 1.41. To investigate the solubility of VF_2 in MgF_2, two small test crystals grown from charges containing 5 and 10 wt% VF_2. The results of x-ray fluorescence analysis and lattice constant measurements for these crystals show that the solubility is at least 9.2 wt% (6.6 mole percent).

Although single crystals have been obtained in almost all the growth runs using the larger system, the overall yield of laser-quality material has been limited because most of the crystals have been cracked. The cracking indicates that the crystals were strained while being cooled to room temperature. Attempts to reduce the strain by reducing the cooling rate have not been successful in preventing cracking, even though in several cases the cooling cycle was extended to more than 10 days. We are currently investigating several other approaches intended to solve the cracking problem, for example, reducing the temperature difference along the length of the crucible and using a seed oriented so that the long axis of the crystal will be perpendicular to the c-axis. Figure III-13 shows a seeded $Co:MgF_2$ crystal grown in this orientation, which minimizes the stress on the crystal produced by the walls of the crucible.

Laser rods up to 5 cm long have been fabricated from crystals of $Ni:MgF_2$, $Co:MgF_2$, and $V:MgF_2$. The long axis of the rods is perpendicular to the c-axis. These rods have very low scattering loss, low strain, and excellent refractive index uniformity. CW laser operation at 77 K has been achieved over tuning ranges of 1.07 to 1.16 μm for $V:MgF_2$, 1.61 to 1.74 μm for $Ni:MgF_2$, and 1.60 to 2.29 μm for $Co:MgF_2$. (See Sec. II-B for details of the laser experiments.)

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A. CHARGE-COUPLED DEVICES: TIME-INTEGRATING CORRELATOR

A CCD implementation of a time-integrating correlator capable of high-speed operation is described in this report. The proposed device will correlate an analog signal with a binary reference, and should find application in spread-spectrum systems. We are currently fabricating a device designed for use with the GPS (Global Positioning System) P-code.

Fig. IV-1. Two principal types of correlators: (a) transversal filter or tapped-delay line and (b) time-integrating correlator.
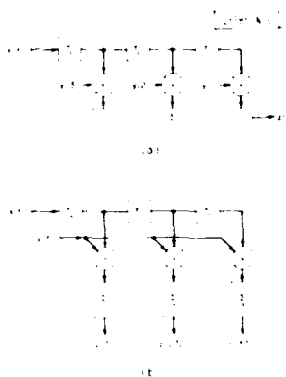
Figure IV-1 shows the two principal types of correlators: (a) a tapped-delay line or transversal filter, and (b) a time-integrating correlator. The CCD literature has concentrated almost exclusively on the transversal filter approach while ignoring the advantages inherent in the time-integrating correlator. We wish to point out in the context of CCD technology the contrasts between these two correlator structures.

The transversal filter has an output data rate equal to the input data rate, and for high-speed applications the bandwidth of the tapping, summing, and detection circuitry becomes the limiting factor. The fastest transversal filter reported to date[1,2] is limited to a 30- to 40-MHz clock rate by the bandwidth of the on-chip MOSFET detection circuit. The time-bandwidth product (TB) of this device is one-half the number of taps.

The time-integrating correlator, in contrast, uses a time-varying reference, $y(t)$, and integrates the product of the signal, $x(t)$, and reference waveforms at each tap over an arbitrarily selected time period. The integrated outputs are then the cross-correlation of $x(t)$ and $y(t)$ for phase-shifts between x and y which vary in units of T_c. The TB product in this case is one-half the input clock frequency $(1/T_c)$ times the integration time, and can therefore be varied.

Two additional advantages of the time-integrating correlator should be mentioned. For programmable transversal filters reported to date, the tap weight values are programmed by digital logic, and a mixed CCD/digital fabrication process is required. The time-integrating

correlator requires no digital storage of the reference waveform, thereby removing a major source of power dissipation from the chip and relieving certain fabrication constraints imposed by the logic.

A second major advantage of a time-integrating correlator concerns errors and the possibility of post-processing to improve device accuracy. The principal errors we would expect in the CCD correlators are g. ..nd offset errors in the tap weight values (charge transfer loss in the delay line should be negligible with current technology). In the transversal filter such errors become convolved with the signal, and to unravel such errors by post-processing of the output is generally impractical, particularly at high data rates. In the time-integrating correlator each output bears only the gain and offset errors of one tap/integrator, and Smythe and Ralston[3] have demonstrated for a SAW/CCD time-integrating correlator a method of reducing these errors which is applicable to this device. Such errors also can be removed with a modest amount of off-chip digital circuitry including a multiplier, an adder, and some memory. Such post-processing is now common, for example, in dealing with the severe pattern noise problems found in most staring infrared imagers.

The goal for our CCD implementation of a time-integrating correlator (illustrated in Fig. IV-2) is a structure capable of the highest possible bandwidth, and to that end we have adopted the "pipe-organ" structure used in high-speed transversal filters.[1,2] In this approach
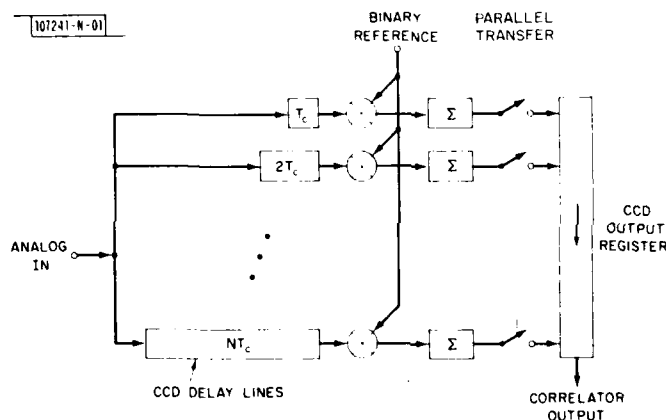
Fig. IV-2. Basic architecture of the proposed high-speed CCD time-integrating correlator. The structure uses a bank of CCD delay lines in the pipe-organ configuration with a binary charge multiplier and integrating well at each delay-line output. Integrated charge is multiplexed onto another CCD to be read out.

the tapped-delay line is replaced by a bank of delay lines with a common input so that the outputs of the pipe-organ represent samples of the analog input at different delay times. Though functionally equivalent to the tapped-delay line, it differs in that the output charge has been generated by a voltage-to-charge conversion and CCD transport which are both high-speed processes. The tapped-delay line by contrast is compromised in speed by the circuitry needed to sense current or voltage at each tap. Because the delay-line signals are charge packets, it is straightforward to perform the binary multiplication by using a gate which, depending on its bias, allows

charge to pass to the integrator or diverts it to a charge dump. The integrator is a CCD storage well or capacitor, and at the end of the integration period the accumulated charge packets are multiplexed into a CCD output register.

Figure IV-3 describes some further refinements to the device which are necessary in order to avoid signal- and code-dependent offsets in the correlator output. For the CCD input where the signal voltage $V_s(t)$ is converted to charge, we use a structure which produces two charge
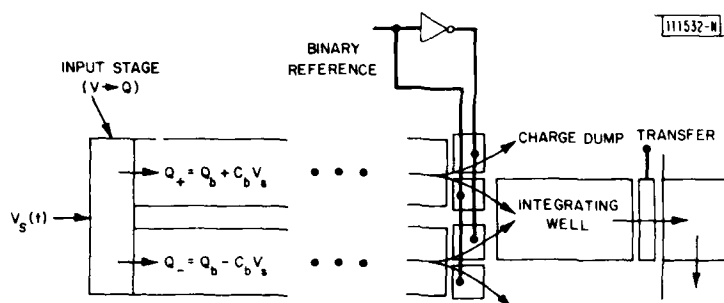
Fig. IV-3. Details of one channel of the correlator. An input structure which creates complementary charge packets and a balanced binary multiplying method are needed to obtain true correlation free of signal- and reference-dependent offsets.

packets, $Q_{\pm} = Q_b \pm C_o V_s$, representing the signal and its complement where Q_b is a bias charge and C_o is a gate capacitance. At the delay-line output a set of four gates controlled by the binary reference and its complement are used to direct charge either into the integrating well or to a charge dump. A high-voltage level on the gate allows charge to pass under it, while a low level blocks it. Thus one of the two charge packets, $Q_{\pm}$, is always directed to the integrator, while the remaining packet is diverted into a charge dump. The action of these gates amounts to a multiplication of each packet by 0 or 1, but we wish to view it in terms of the desired reference function $R(t) = \pm 1$. With $R = +1$ and -1 corresponding to high and low levels, respectively, for the binary reference, we see from Fig. IV-3 that Q_+ is multiplied by $(1 + R)/2$ and Q_- by $(1 - R)/2$. The expression for the integrated charge, after N clock periods and with an M-stage delay line, is then

$$Q_o = \sum (Q_b + C_o V_s)(1 + R)/2 + (Q_b - C_o V_s)(1 - R)/2$$

$$= NQ_b + C_o \sum_{n=1}^{N} V_s[(n - M)T_c] \cdot R(nTc) \quad .$$

The output signal is therefore the desired correlation plus a fixed bias charge.
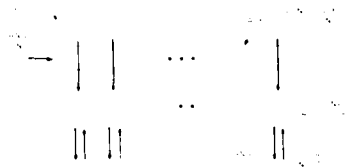
Fig. IV-4. A CCD parallel-processing architecture where computations involving analog sampled data are done in the charge domain and large numbers of data points are processed in parallel.
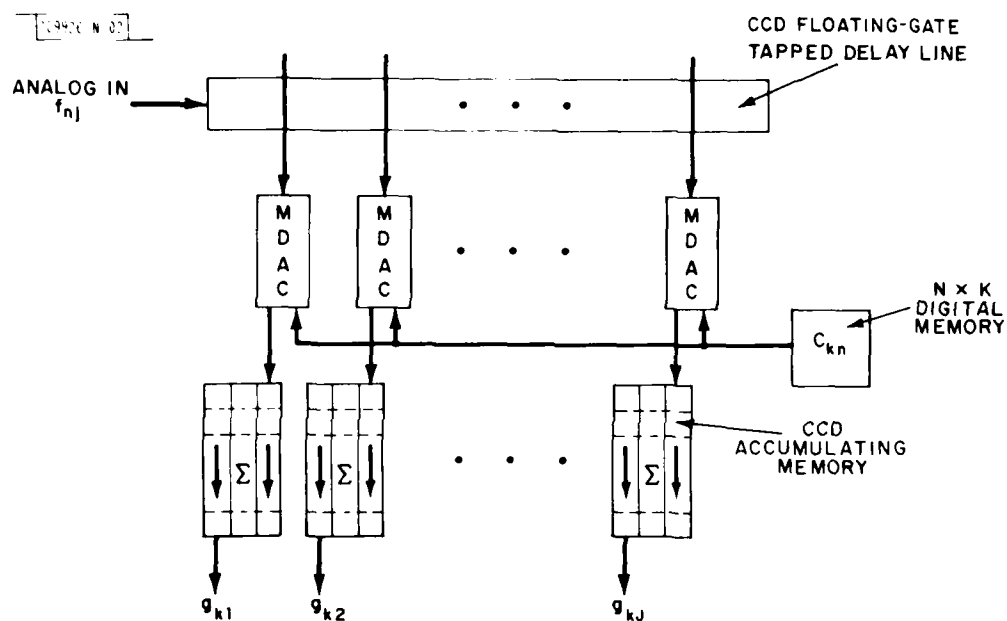
A GENERAL PURPOSE MATRIX-MATRIX PRODUCT DEVICE

$$g_{kj} = \sum_{n=1}^{N} c_{kn} f_{nj} \text{ , FOR } k = 1, 2, \dots K, \ j = 1, 2, \dots J$$

Fig. IV-5. A CCD matrix-matrix product device which computes the function [G] = [C][F], where the F matrix elements are analog sampled data and the C matrix elements are digital numbers.

We are currently fabricating a 32-stage time-integrating correlator for use with the GPS P-code. This code has a clock rate of 10.23 Mbps. The correlator will be clocked at 20.46 MHz and therefore provide 16 early and 16 late correlations spaced one-half code bit apart.

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D. L. Smythe

B. CHARGE-COUPLED DEVICES: A NEW PARALLEL-PROCESSING ARCHITECTURE

A new CCD parallel-processing architecture is described. With this architecture, devices can be built to perform many high-level mathematical operations such as vector-matrix, matrix-matrix, and triple-matrix products. Possible applications for devices implementing these functions are evaluation of discrete Fourier transforms, radar signal processing, and two-dimensional image processing. The basic device structure (shown in Fig. IV-4) consists of a floating-gate CCD tapped-delay line and an array of CCD signal processors. The delay line is for shifting and holding analog sampled data, which are in the form of charge packets. At each stage of delay a floating-gate sensing electrode is coupled to a corresponding CCD signal processor, and the sampled data are transferred and subsequently processed in parallel. Within each processor all the computation functions are performed in the charge domain, and local charge-domain memories are included for storing the processed signal. Based on this generic device architecture, a matrix-matrix product device and a triple-matrix product device have been designed and are described below.

A schematic of a matrix-matrix product device is shown in Fig. IV-5. This device is capable of computing the function

$$g_{kj} = \sum_{n=1}^{N} c_{kn} f_{nj} \quad for \ j = 1,2,....,J, \ k = 1,2,....,K .$$

where f_{nj} are sampled analog data and c_{kn} are digital numbers. It consists of a J-point, floating-gate, tapped-delay line; J M-bit charge-domain multiplying D/A converters (MDACs); J K-stage CCD accumulating memories, each with separate input and output shift registers; and a digital memory for N-by-K, M-bit words. The digital memory can be either on-chip or off-chip. All the MDACs have common digital inputs, but the output of each MDAC goes to a corresponding accumulating memory, as shown in Fig. IV-5.

We are in the process of designing a CCD matrix-matrix product device with N, K, and J chosen to be 32. The chip size is estimated to be 30,000 mil^2 excluding the digital memory. At a 10-MHz clock rate, the device is performing the equivalent of 3.2×10^8 m-bit $\times$ m-bit digital multiplications and 10^{10} additions/second.

The schematic of a triple-matrix product device is shown in Fig. IV-6. The device calculates the function

$$h_{k\ell} = \sum_{j=1}^{J} g_{kj} d_{j\ell}$$

where

$$g_{kj} = \sum_{n=1}^{N} c_{kn} f_{nj} \quad .$$

It can be seen that the top part of the device (i.e., the tapped-delay line, the MDAC's, the accumulators, and the digital memory) is identical to the previously described matrix-matrix product device. The lower part of the device consists of an I -by-K fixed-weight CCD multiplier bank. All the fixed-weight multipliers on the same column have a common analog input (i.e., the output from the jth accumulating memory is coupled to the inputs of the jth column of the fixed-weight multipliers). All the multipliers on the same row have a common output node.

The chip area of a CCD triple-matrix product device with J, K, 1, chosen to be 16, is estimated to be 35,000 mil^2. At a 10-MHz clock rate, the fixed-weight multiplier bank is performing 2×10^9 m-bit × m-bit multiplications/second.

In summary, a new CCD parallel-processing architecture is described which allows us to build CCD devices with enormous computation power. We have achieved this by keeping the signal and performing the computation in the charge domain, and processing large numbers of sampled data in parallel.

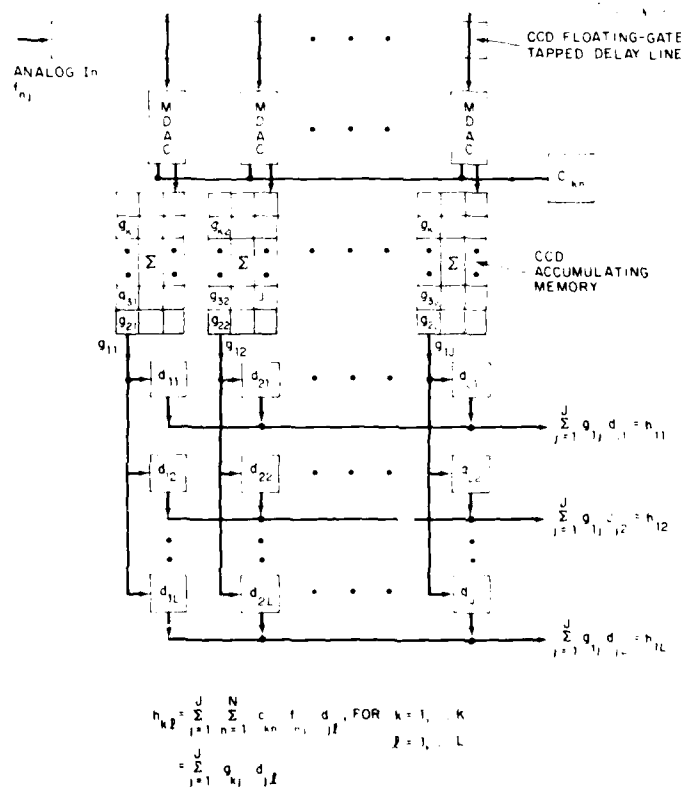<div align="right">A. M. Chiang</div>

Fig. IV-6. A CCD triple-matrix product device which computes the function [H] = [G] [D] = [C] [F] [D], where the F matrix elements are analog sampled data and the C and D matrix elements are digital numbers.

C. CHARACTERIZATION OF A BCl₃ PARALLEL-PLATE PLASMA SYSTEM
FOR ALUMINUM ETCHING

The etching of aluminum on oxidized silicon substrates with a boron trichloride (BCl_3) plasma has been studied. Process parameters have been optimized to provide clean, vertical walls without residue. Techniques to maintain constant plate-to-plate voltage rather than constant power are utilized, and nonstandard geometries are employed. Plate-to-plate voltage dependence on power, gas flow, load, and electrode temperature has been characterized for the system along with the dependence of plate-to-plate voltage on system configuration. Top plates of various design used at several separation distances were found to produce variations in uniformity of etch.

The impetus toward ever-finer lines in aluminum interconnects for VLSI is the driving force in developing dry-plasma-processing technology. For our experiments a modified version of a plasma-etching system (Fig. IV-7) reported by Herndon and Burke[4] was used. Our system has larger capacity and has added electrode water cooling. BCl_3 is used as the etch gas because of its ability to etch through the native oxide layer[5,6] and its resistance to polymer formation in a stainless-steel system, in contrast to CCl_4. Samples in these experiments were 2-in.-dia. silicon wafers with 1-μm-thick aluminum on 2000-Å-thick SiO_2. The aluminum is evaporated using an induction-heated source. Positive photoresist 2 μm thick patterned into both large geometries and gratings with periods varying from 4 to 20 μm is used as the etch mask.

Plate-to-plate voltage was varied for different top-plate geometries to optimize the process. When maintaining constant power density, large plate-to-plate voltage variations were seen with
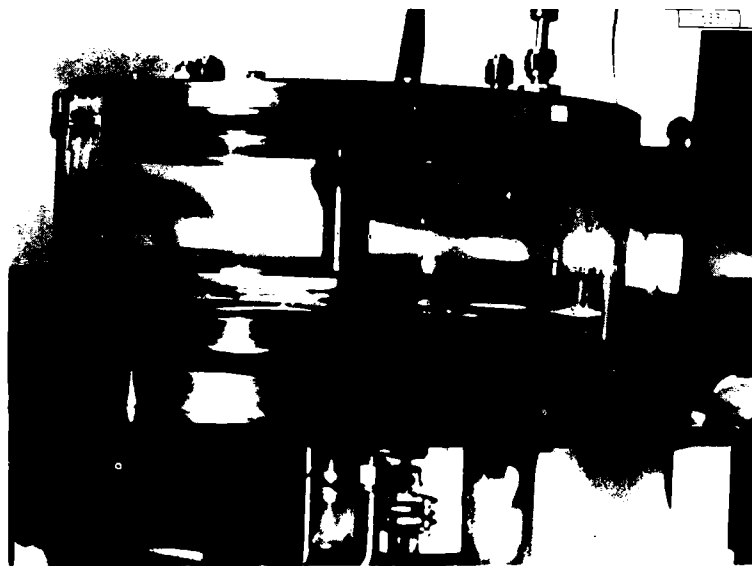

Fig. IV-7. Parallel-plate system for aluminum etching. Plate-to-plate separation is 7/8 in.; the large (11-in.-dia.) top electrode is shown here. The system is stainless steel and pyrex. Gas enters at top right of chamber, goes around the edge of the top plate, and is pumped out through the exhaust hole in the bottom electrode.
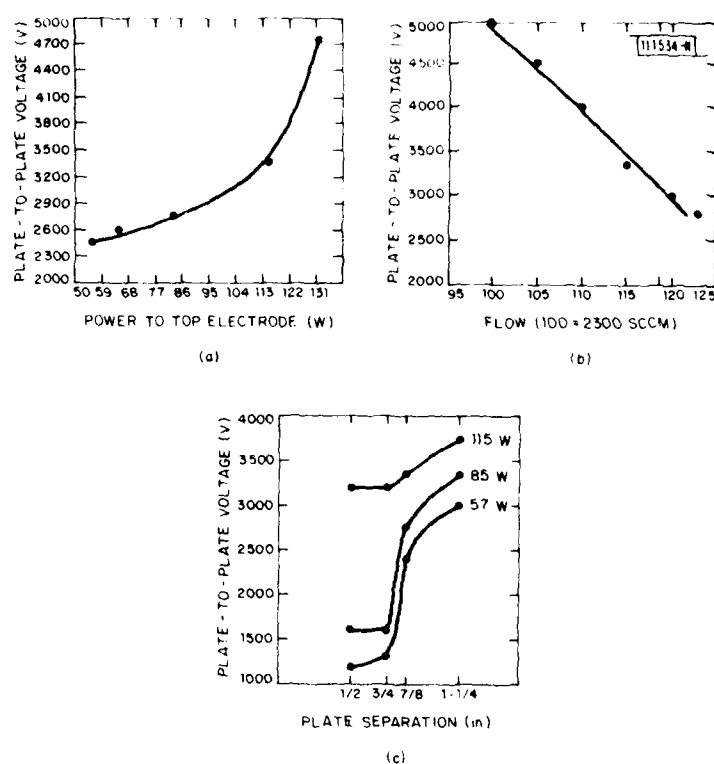
Fig. IV-8. Plate-to-plate voltage dependence on (a) power (7/8-in. plate separation), (b) flow (7/8-in. plate separation, 175 W to top electrode), and (c) plate separation. All measurements were made with the small (7-1/4-in.-dia.) stainless-steel top electrode.

changes in plate separation (as indicated in Fig. IV-8), resulting in major changes in the etching process. The plate-to-plate voltage was then characterized with respect to other parameters (pressure, gas flow, power, etc.) to optimize both etch rate and etch uniformity.

The bottom plate for the system is shown in Fig. IV-9. A top plate that covers only ~3/4 of each 2-in. wafer (see dotted line in Fig. IV-9) gives a uniform etch across the wafer. Planetary motion is necessary for good uniformity in this configuration. Several other top plates have been studied, but the top plate that only partially covers the samples gives best uniformity. The variation in etch uniformity with system geometry is probably due to either a change in gas flow *dynamics due to a change in plate size*, or a change in the electric field when plate configuration is changed.

BCl_3 plasma etching produces aluminum lines with vertical sidewalls and minimal undercut. Rinsing with H_2O immediately after removal from the chamber appears to clean up any black corrosive residues which form during the etching. One persistent problem, however, is the appearance of an additional spongy residue on the SiO_2 layer after the aluminum has been etched away. Auger analysis shows significant amounts of carbon present in this film, as well as some chlorine and boron. Scanning electron micrographs of both types of residue are shown in Fig. IV-10. While an H_2O rinse removes the black corrosive residue, it hardens the spongy

Fig. IV-9. Bottom plate of etching system. The whole plate rotates clockwise, and each of the 6 wafer holders rotates clockwise. The exhaust hole is at the center. The circle drawn on the photo indicates the area of the wafers covered by plasma when the small, 7-1/4-in.-dia. stainless-steel top electrode is used.
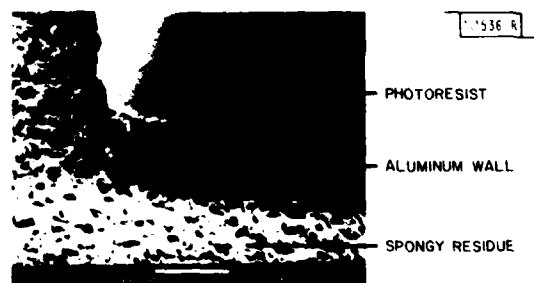
(a)
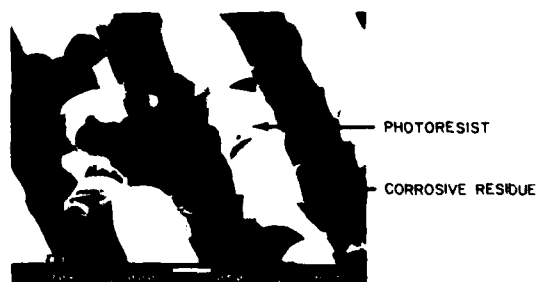
(b)

Fig. IV-10. Samples plasma-etched approximately 24 min. in BCl₃. (a) Carbon left on surface after etch, which is removed with O₂ plasma and (b) black corrosive residue usually seen on areas where aluminum is not completely etched away. Residue can be removed with H₂O rinse.

(a)

(b)
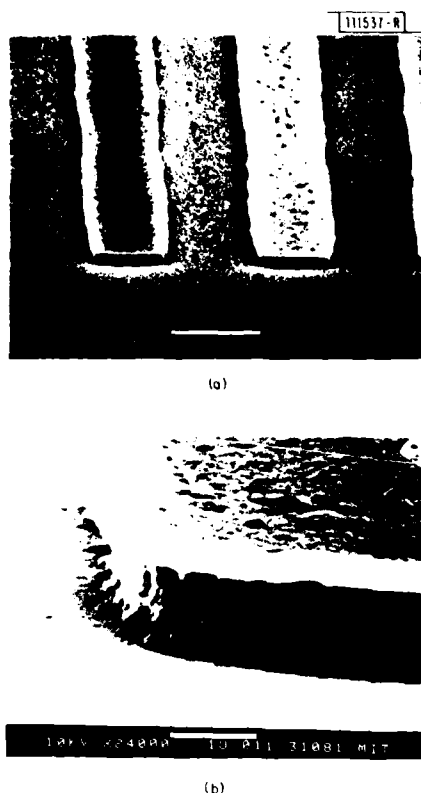
Fig. IV-11. Aluminum, 1 μm thick, etched 17-1/2 min. in BCl_3 with small top electrode, followed by O_2 plasma clean. Surface is clear of residue, and the amount of undercut is small. A thin layer of positive photoresist is still on top of the aluminum lines. (a) X2,400, (b) X24,000.

residue, making it more difficult to remove. A CF_4 and/or O_2 in situ post-etch plasma process will remove both types of residue. A sample that has received an O_2 plasma is shown in Fig. IV-11. We have determined that the carbon is derived from the positive photoresist. Work is in progress to determine if alternative masking materials will have an effect on the formation of residues.

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D. J. Silversmith
R. W. Mountain

D. HIGH-RESOLUTION PATTERNING OF SILICON WITH $SiCl_4$ REACTIVE-ION ETCHING

Anisotropic etching of silicon in a reactive plasma is becoming increasingly important for the formation of high-resolution patterns for VLSI. This process, however, is often made difficult by a relatively high mask etch rate. Recently, Ho..vitz[7] reported the directional etching of deep structures in silicon using Cl_2-containing gases in a reactive-ion etching system. In particular, very high silicon/mask etch-rate ratios were obtained using $SiCl_4$ and controlled amounts of O_2. Here we report the etching of very fine (3200-Å-period) structures in silicon using an $Ar/SiCl_4/O_2$ gas mixture, with aluminum and nickel as the etch mask materials.

Aluminum patterns on silicon were formed using laser holographic exposure of positive photoresist followed by chemical etching of 400-Å-thick aluminum. In addition, both 800-Å-thick

aluminum gratings and 400-Å-thick nickel gratings were made by x-ray exposure of PMMA on silicon, followed by deposition of the appropriate metal and lift-off. The grating period in each case is 3200 Å.

The reactive-ion etching system used has been described elsewhere.[7] A 20:1:1 gas mixture of $Ar/SiCl_4/O_2$ was used, and the samples were placed on an SiO_2 target. Chamber pressure during the runs was 20 mTorr, and peak-to-peak voltage was maintained at 1.1 kV.

SEM photos were used to evaluate the etch process. Directional etching was achieved with profiles similar to those seen by Horwitz on larger (>1 μm) features. Figure IV-12 shows the aluminum-masked sample patterned with laser holographic exposure. The etch was anisotropic
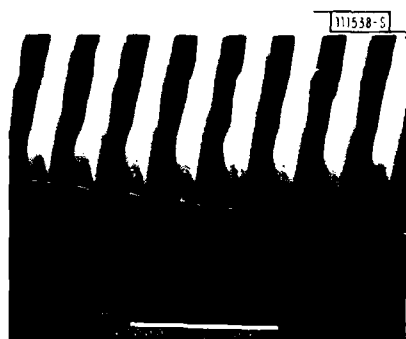
Fig. IV-12. 3200-Å-period grating etched in silicon using 400-Å-thick aluminum mask formed by holo- graphic exposure and wet chem- ical etching. Sample was etched 10 min. in 20:1:1 $Ar/SiCl_4/O_2$; ap- proximately 5600 Å silicon was etched.

Fig. IV-13. 3200-Å-period grating etched in silicon using 400-Å-thick nickel mask formed by x-ray ex- posure of PMMA and lift-off. Sam- ple was etched 10 min. in 20:1:1 $Ar/SiCl_4/O_2$. The nickel mask has been etched away.

and left a smooth etched silicon surface. The grooves are approximately 5600 Å deep, and the aluminum mask remains intact. Figure IV-13 shows the nickel-masked sample. The tops of the lines show that the mask first eroded at the edges, then was etched away completely. The sidewalls, however, are vertical and the etched surfaces are smooth. Figure IV-14 shows the aluminum-masked sample patterned by x-ray exposure and lift-off. The 6400-Å-deep grooves have a "keyhole"-type cross section. This effect is thought to occur because of redeposition of SiO_2 on the slow-etching surfaces (the aluminum mask). The SiO_2 comes from sputtering of the substrate platform and from the reaction of Si and O_2 in the gas phase. During the etching process, this deposition tends to enhance the unetched (mask) line-width, which in turn results in narrowing of the etched groove at the base. While the lines in Fig. IV-12 also appear to have the keyhole-type cross section, the effect is not as pronounced with the thinner, wet-etched aluminum mask. For the experimental conditions described here, the redeposition phenomenon associated with the slow-etching surface seems to occur only for the aluminum-masked sample and not for the nickel, although their etch rates are similar. Etch rates for aluminum, nickel, and silicon are given in Table IV-1.
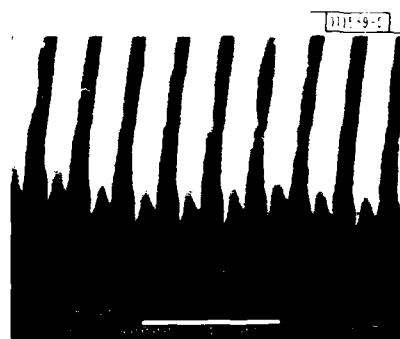
Fig. IV-14. 3200-Å-period grating etched in silicon using 800-Å-thick aluminum mask formed by x-ray exposure of PMMA and lift-off. Sample was etched 10 min. in 20:1:1 $Ar/SiCl_4/O_2$. The aluminum mask is intact, with SiO_2 deposition visible on top of the mask.

TABLE IV-1

REACTIVE-ION ETCH RATES*

	Å/Minute
Silicon	600
Aluminum	42
Nickel	45

* Using a 20:1:1 mixture of $Ar/SiCl_4/O_2$: system pressure of 20 mTorr; and peak-to-peak voltage of 1.1 kV.

Additional experiments are being performed to maximize the silicon-to-metal etch-rate ratio while maintaining the desired profile. Use of the selective deposition of SiO_2 to improve our masking capabilities is being investigated. Also, we intend to characterize the quality of the etched surfaces via both optical and electrical measurements. If the reactive sputter etching process produces little or no damage, this technique should prove valuable in the fabrication of the silicon permeable base transistor.

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S. Cabral   N. Efremow
J. Melngailis

E. ELECTRON-BEAM TESTING AND RESTRUCTURING OF INTEGRATED CIRCUITS

Wafer-scale integrated systems could become practical if sophisticated techniques are developed for locating defective subsystems on each wafer and restructuring the subsystems and interconnections to compensate for these defects. In order to perform functional testing one must be able to alter and sense logic states internal to the integrated system. To restructure an integrated system, nonvolatile switches would be opened or closed to provide customization (e.g., the bit pattern in a PLA or ROM) or fault-avoidance.

Techniques have been developed for providing input injection, output sensing, and nonvolatile restructuring using an electron beam.[8,9] The electron-beam techniques were selected to be compatible with a commercially available electron-beam lithography system and with standard nMOS processing. In order to demonstrate the feasibility of the proposed techniques and to detect unforeseen practical problems, nMOS test structures including an electron-beam switched latch, an electron-beam multiplexer, floating-gate transistors, and simple FETs were designed, fabricated, and tested.

Output sensing has been demonstrated using both an electron-beam multiplexer circuit and voltage-contrast techniques. Because of poor secondary-electron-collection efficiency in our

LEBES (Electron-Beam Lithography System), the voltage-contrast technique yielded logic sensing rates of only ≈100 Hz. However, theoretical predictions and experimental measurements indicate that a bandwidth >1 MHz is feasible if an optimized detector is constructed. Logic sensing times as short as 2 µs have been demonstrated using the electron-beam multiplexer, and bandwidths >20 MHz appear feasible.

Logic states have been altered with electron-beam pulses as short as 300 ns, and input clock rates in excess of 100 MHz may be possible. Electron-beam control of nonvolatile links has been achieved using two techniques: (1) inducing large threshold shifts in MOSFETs by electron bombardment of the gate oxide and (2) electron storage on floating-gate FETs. These switches have been programmed in times < 1 ms, and programming times in the microsecond range are feasible. Both types of nonvolatile links can be toggled "on" and "off" under electron-beam control. The floating-gate devices exhibit excellent retention characteristics and are promising electron-beam-controlled nonvolatile switches.

<div align="right">D. C. Shaver</div>

F. POLYIMIDE-BASED INTERCONNECT TECHNIQUE ON GaAs

High-density, high-frequency microcircuits place increasing burdens on interconnect technology. Significant strides are being made in monolithic GaAs integrated circuits at microwave frequencies. To reach their full practical potential, these circuits will require conceptual innovation in the interconnect scheme, both on the chip and between chips. No longer will wire or ribbon bonds be appropriate. We report the development of a new interconnect technique which is directly applicable to discrete, surface-oriented[10] GaAs mixer diodes. This technique should preserve the high performance of previous mixers yet obviate the need for laborious whisker contacting[11] or hybrid mounting[12] of the diode. When fully developed, this fabrication process should offer the advantages of reduced cost and increased ruggedness of heterodyne receivers and other monolithic devices.

The technique incorporates the use of polyimide as a conformable dielectric on which a microstrip line is photolithographically defined. This microstrip circuit would allow direct embedding of the mixer into its waveguide environment. The fabrication process was demonstrated on mechanical samples of semi-insulating GaAs, approximately 375 µm thick. A typical GaAs device metallization (e.g., Ti/Au) is first sputtered on the polished side, as shown in Fig. IV-15. The appropriate planar device structure would then be photolithographically defined and chemically etched. For this demonstration, a planar slot antenna feed to the mixer region was delineated. Also, 250-µm-dia., 125-µm-deep holes, which later serve as front-to-back alignment marks, are chemically etched as shown in Figs. IV-15 and -16. Thin polyimide layers have been used in the past for multiple-layer metallization of silicon chips. Our application requires thick polyimide. First, the adhesion promoter was spun on the wafer and baked at 100 °C for 1 h, then 4 µm of polyimide was spun on and the wafer was baked at 80 °C for 1/2 h. The process was repeated until approximately 12 µm of polyimide was applied. Final imidization was done at 350 °C for 1 h in N_2. The resulting thickness of polyimide was approximately 8 µm, indicating a 35-percent shrinkage of the polyimide during cure.

A second Ti/Au/Ti metallization is sputter deposited and a 50-µm-dia. window is defined and chemically etched through the metallization directly over the 75-µm-dia. device ohmic contact. By means of reactive-ion etching in an O_2 atmosphere, the exposed polyimide was removed until the simulated ohmic contact was reached, as shown in Fig. IV-15. By sputtering
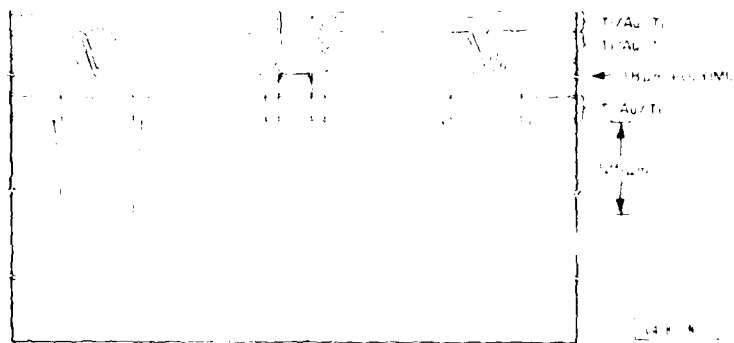
Fig. IV-15. Schematic side view of a GaAs wafer with front-to-back
alignment holes, metallization, and polyimide.

Fig. IV-16. The top view of a GaAs wafer
with separation channels, front-to-back
alignment holes, and overlay pattern of
monolithic mixers.

58

a third Ti/Au/Ti sandwich over the entire wafer, direct electrical contact is established to the ohmic region of the simulated mixer through the polyimide window. Microstrip line of 50-ohm impedance is now fabricated as shown in Fig. IV-17. This concludes the work on the active (device) side of the wafer.

Fig. IV-17. The microstrip atop the polyimide. Direct electrical contact is made to the ohmic region.

The back side is chemically etched until the front-to-back alignment holes become visible. A protective mask is then applied which will protect the GaAs on the back side of the device. The chemical etching is resumed until the gold layer adjacent to the GaAs is exposed. Etching the GaAs not only defines the GaAs chip size and forms an easily contacted cantilever ground plane, as evident in Figs. IV-17 and -18, but also eliminates any saw cutting of the wafer. In our initial attempt, photoresist was used as this etch-through mask, and it did not stand up to the long etch. A subsequent refinement using pyrolytic SiO_2 has proved quite resistant.[13]
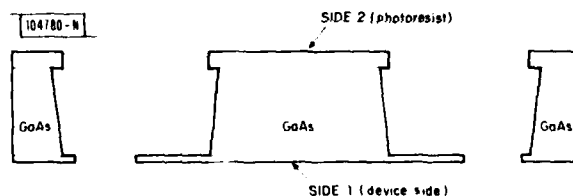

Fig. IV-18. Schematic of etch-through and separation of the individual chips from the wafer.

We have shown it possible to use polyimide as a dielectric to form microstrip for interconnecting small areas where delicate wire-bonding techniques are tedious and may thus cause low yields of packaged devices. Furthermore, field replacement by the user becomes feasible, a clear advantage in contrast to the current practice of returning the mounted diode to the original fabricator for whisker contacting. Variations of this polyimide technique are being considered for use in superconducting devices. Studies and experimentation on the properties of polyimide at high frequencies and low temperatures in working devices will be reported later.

W. Macropoulos
R. A. Murphy

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V. ANALOG DEVICE TECHNOLOGY

A. A SHORT PEDESTAL-OF-DELAY, VERY LOW FEEDTHROUGH SAW FILTER

The use of very short pedestal-of-delay surface-acoustic-wave (SAW) filters has been limited because of the large direct electrical feedthrough which is unavoidable when a conventional interdigital input transducer is positioned close to the output transducer. The feedthrough is a result of fringing fields both in the substrate material and through the space above the substrate. Feedthrough can be substantially reduced using edge-bonded transducers (EBT),[1] which we have reported previously. Figure V-1 shows the basic structure of an EBT. The indium film which bonds the LiNbO$_3$ transducer to the SAW substrate serves as the ground plane of the EBT. The ground plane in turn terminates the electric fields which are responsible for the electric-to-acoustic transduction in the EBT. Thus, fringing fields in the SAW substrate are minimized so that the structure of the EBT inherently provides low feedthrough. Furthermore, because electrical connection to the EBT is below the surface of the SAW substrate, a ground plane can be positioned arbitrarily close to the substrate and parallel to it. The ground plane can then intercept the residual fringing fields above the EBT. Fringing fields in conventional interdigital transducer (IDT) designs are substantially higher both in and above the SAW substrate. Figure V-2 shows schematically the IDT and EBT designs and illustrates how feedthrough can be reduced.

To test and quantify the low-feedthrough design, we have fabricated a device with a LiNbO$_3$ EBT on an ST-quartz substrate. A 19-finger-pair IDT was fabricated on the surface of the quartz at a distance of about 30 μm from the EBT. This yields a pedestal-of-delay of 10 ns. Feedthrough in the device has been further suppressed by the use of a balanced, dual-track design, shown in Fig. V-3. The acoustic beam is divided into two tracks which are driven with a phase shift of 180° relative to one another. The two tracks of the IDT are physically displaced one-half period, or 180°, at center frequency. The electrical signals at the output of the two transducers are thus in phase and can be added together by using a sum-difference hybrid. As can be seen in the figure, however, the direct electric feedthrough will produce voltages of opposite phase on the IDT electrodes of the two tracks. Thus the feedthrough will appear only on the difference port of the sum-difference hybrid, and a further suppression of feedthrough is gained.

The results of the ST-quartz device are shown in Fig. V-4 which is a multiple-exposure photograph of the oscilloscope. The top trace shows the input impulse and the bottom trace shows the device output. In the middle trace the device has been replaced by a 110-dB attenuator. The middle trace serves to calibrate the measurement system delay (amplifiers, cables, etc.) and gain. One can see that the acoustic wave delay is approximately 10 ns. At that point, the bottom trace goes well off scale at the oscilloscope gain setting where the direct feedthrough is visible. It can also be seen that the feedthrough level is nearly 110 dB lower than the input level. Figure V-5 shows more of the device output. The top trace is the input impulse, the bottom trace is the output at the same gain setting as in Fig. V-4, and the middle trace is the output with an extra 70-dB attenuation.

The techniques described here will be applied to a SAW/CCD (charge-coupled device) structure to produce a programmable tapped-delay line with a 10-ns pedestal-of-delay. The structure will consist of a LiNbO$_3$ EBT on a LiNbO$_3$ delay-line air-gap coupled to a Si CCD. The use of
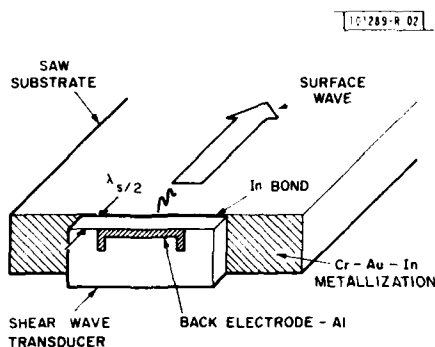
Fig. V-1. Basic structure of edge-bonded transducer.
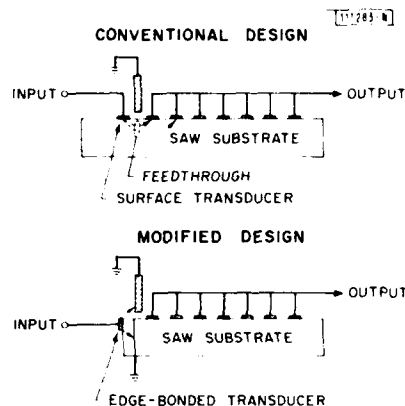
Fig. V-2. Schematic cross-sectional view (top) of conventional tapped-delay-line design and (bottom) edge-bonded-transducer design showing how fringing electric fields are suppressed in latter.
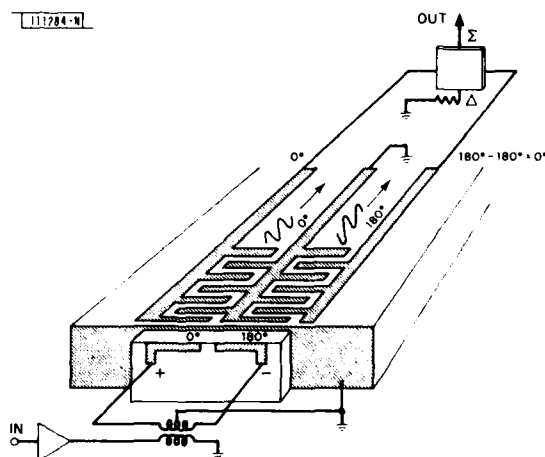
Fig. V-3. View of dual-track delay-line design. Indicated on the figure are the phases of the acoustic signals. Inspection of the geometry shows that the two output connections will tend to have opposite polarity for any residual feedthrough and the same polarity for the desired output. Thus the feedthrough will appear at the difference port of the hybrid, while the desired output will appear at the sum port.

Fig. V-4. Oscillogram. Top: input impulse; bottom: device output at high gain setting showing feedthrough; and middle: calibration trace with 110-dB attenuator in place of device.

Fig. V-5. Oscillogram over longer time scale than in Fig. V-4. Top: input impulse; bottom: device output showing feedthrough; and middle: same as bottom trace but signal attenuated by 70 dB.
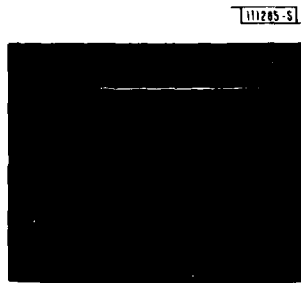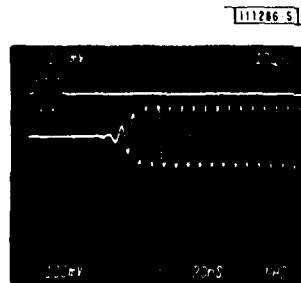
a CCD, rather than an IDT, allows rapid programmability of the filter characteristics, as has been previously described.[2] To produce a practical device it is estimated that 100 dB of feedthrough isolation is needed in this structure for adequate dynamic range.

D. E. Oates

B. CONSIDERATIONS FOR AN INTEGRATED OPTICAL SPECTRUM ANALYZER

A spectrum analyzer with a wide instantaneous bandwidth, but with simultaneous narrow frequency resolution, is a desired component. Optical spectrum analysis is one approach. Recently several papers[3-8] concerned themselves with the development of an integrated optical spectrum analyzer (IOSA). To date the performance of IOSAs has fallen far short of design goals and the performance achieved with bulk devices. The device consists of four basic elements: (1) an input lens, (2) a Bragg cell (either surface- or bulk-acoustic wave), (3) an output lens, and (4) a detector array. Below are addressed some of the design problems involved with the input lens and output detector array.

1. Limitations of the Detector Array

We begin with the detector array since it is the most limiting component in terms of theoretical performance achievable. The detector array is typically an array of photodiodes with a CCD readout or a direct CCD detector array. The main parameters to consider for the detector array are (a) dynamic range and (b) detector element size.

From signal-processing considerations the spectrum analyzer dynamic range should be at least 10 dB greater than the time-bandwidth (TB) product. In practice, direct-detection photodiode arrays are limited to a maximum dynamic range of about 80 dB (Ref. 9). Thus the spectrum analyzer dynamic range is limited to around 40 dB. This limits the maximum useful TB product of an IOSA to approximately 1000 (30 dB).

A practical detector array is limited to approximately 10-μm pitch.[5] The size of the detector elements directly influences the resolution achievable by the spectrum analyzer. If the pitch

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of the array is P and each detector is one resolution element, then the frequency resolution δf is given by

$$\delta f = \frac{n v_a}{F \lambda_o} \, P \tag{V-1}$$

where λ_o is the optical wavelength, n the refractive index, F the focal length of the output lens and v_a the acoustic velocity. A typical IOSA uses $LiNbO_3$ to support both a surface-guided optical wave and a surface acoustic wave. Practical limitations of substrate size, scattering loss, diffraction, etc., limit the focal length F of the output lens. For such an analyzer, if the optical wavelength λ_o = 0.82 μm and F = 3.5 cm, then from Eq. (V-1) we obtain $\delta f \approx 2.7$ MHz for a typical pitch P = 10 μm.

2. Input Lens Design

The input lens is required to collimate input light before passage through the Bragg cell. The design parameters to be addressed are (a) spurious illumination and dynamic range, (b) resolution and crosstalk between adjacent cells, and (c) scalloping loss.

The optical amplitude imaged on the detector array by the output lens is the Fourier transform of the output of the Bragg cell. If the latter amplitude distribution is denoted by W(x), $|x| \leqslant D/2$, the illumination is thus

$$U(f_x D) = \int_{-\infty}^{\infty} du \, W(u) \exp[-i2\pi f_x Du] \tag{V-2}$$

where f_x = $(n/F\lambda_o)$ x' and x' is the beam deflection.[10] The weighting function W(x) is the product of the input weighting of the optical beam, the weighting of the input lens, and any weighting introduced by a nonuniform diffraction efficiency in the Bragg cell.

A uniformly weighted optical beam is undesirable in an optical spectrum analyzer because of the high sidelobe level of the intensity distribution. Consider the case of an ideal detector with uniform sensitivity and no dead spaces between elements. In this case the active element (pel) width p equals the pitch. Figure V-6 shows the normalized optical power into adjacent detector pels as a function of normalized pel width for a uniformly weighted optical beam. For a pel width p = $F\lambda_o/nD$ corresponding to the Rayleigh resolution criterion, the power into adjacent cells (m = 1) is approximately −11 dB and the sidelobes fall off slowly (6 dB/octave), so the spillover into neighboring cells (m = 2, 3, 4) is also significant (>−30 dB). An interfering signal at the maximum input level would thus seriously degrade the ability of the spectrum analyzer to detect weak signals in adjacent channels.

Various weighting functions are compared in Fig. V-7. For each weighting, the null-to-null width w_o of the mainlobe on the detector array in the focal plane is shown together with the crosstalk level into the immediately adjacent detector elements. The calculations assume a pitch p equal to w_o in order to meet the low crosstalk requirements while at the same time minimizing the scalloping loss.
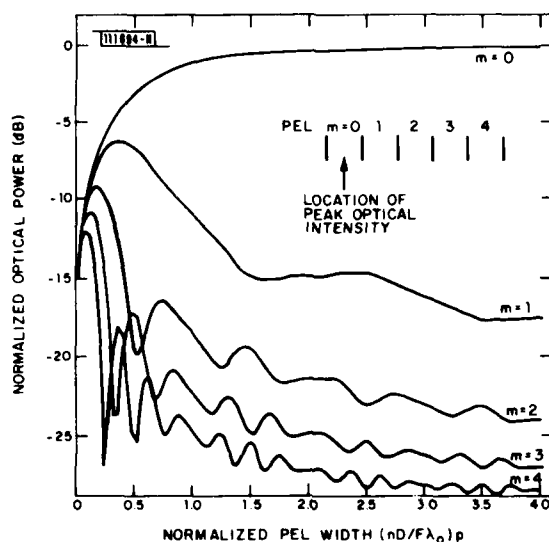
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Fig. V-6. Normalized optical power into the mth-nearest-neighbor detector pels as a function of pel width (uniformly weighted optical beam).

From Fig. V-7 we see that by using an optimum weighting function for a given crosstalk level in decibels, the required array pitch lies approximately on the straight line.

$$P = \frac{F\lambda_o}{nD} [0.96 - 0.069 \text{ (crosstalk level)}] \qquad (V-3)$$

For a typical crosstalk requirement of −30 dB, the frequency resolution of the analyzer is then determined from Eqs. (V-1) and (V-3) to be $\delta f \cong 3/\tau$, where $\tau = D/v_a$ is the acoustooptic inter-action time. From Fig. V-7 we also note that for achieving crosstalk levels $< \sim -30$ dB truncated Gaussian weighting functions are not suitable.

Finally, we consider scalloping loss, the reduction in the detected output that occurs when the center of the mainlobe is located off the center of a pel. This loss is substantial in practical detector arrays which have either dead spaces between pels or substantially nonuniform sensitivity across the pels. To minimize this loss, w_o should be a maximum, consistent with the crosstalk requirement. Thus, for a detector array with dead spaces the optimum system performance will be realized by designing w_o to be equal to the pitch (pel plus dead space). Figure V-8 shows the maximum detector scalloping loss as a function of dead-space/pel ratio for a Gaussian beam truncated at 1.3 times the 1/e width (T = 1.3). The adjacent cell crosstalk level is <−30 dB (see Fig. V-7). For comparison, curves are shown in which the null-to-null beam-width is equal to the pitch (a) and also for which the null-to-null beamwidth is simply equal to the pel width (b). The former choice is clearly seen to be superior, and furthermore the re-quired optical aperture is less. Figure V-8(c) also shows the scalloping loss dependence for a nonoptimum truncated Gaussian weighting (T = 1, null-to-null width equal to pel width), which is unfortunately typical of that used in existing and proposed IOSAs.[4, 5, 11]

P. V. Wright

1 RECTANGULAR
2 COSINE
3 COSINE SQUARED
4 RIEMANN
5 HAMMING
6 GAUSSIAN
 (truncation ratio, T = 1.0)
7 GAUSSIAN (T = 1.1)
8 GAUSSIAN (T = 1.2)
9 GAUSSIAN (T = 1.3)
10 GAUSSIAN (T = 1.4)
11 GAUSSIAN (T = 1.5)
12 GAUSSIAN (T = 1.6)
13 KAISER-BESSEL
 (-30-dB sidelobe)
14 KAISER-BESSEL
 (-35-dB sidelobe)
15 KAISER-BESSEL
 (-40-dB sidelobe)
16 TAYLOR
 (-30-dB sidelobes)
17 TAYLOR
 (-35-dB sidelobes)
18 TAYLOR
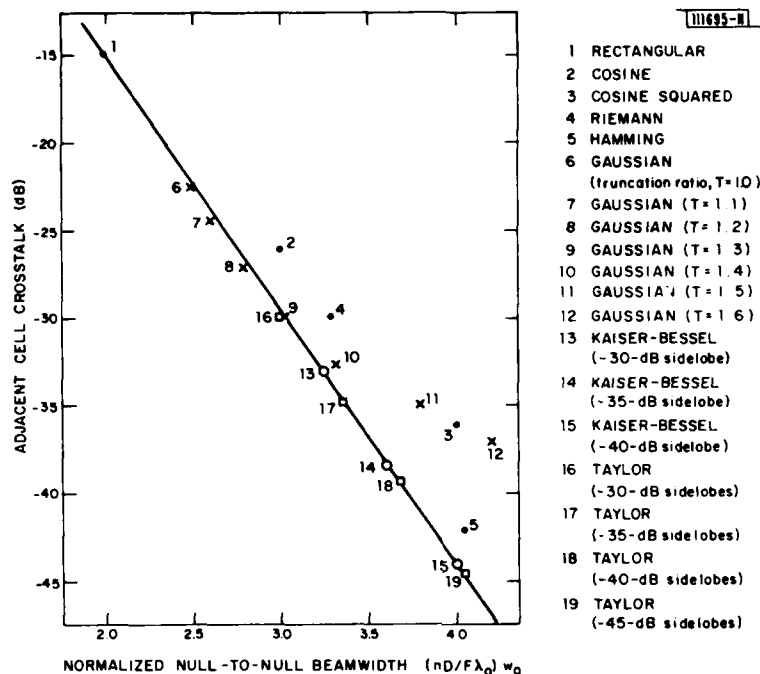 (-40-dB sidelobes)
19 TAYLOR
 (-45-dB sidelobes)

Fig. V-7. Adjacent cell crosstalk vs null-to-null beamwidth for various weighting functions.

Fig. V-8. Maximum scalloping loss vs dead-space/pel ratio for optimum and nonoptimum Gaussian weighting functions: (a) truncated at $1.3 \times 1/e$ width, null-to-null width equals pitch; (b) truncated at $1.3 \times 1/e$ width, null-to-null width is pel width; and (c) truncated at $1/e$ width, null-to-null width is pel width.
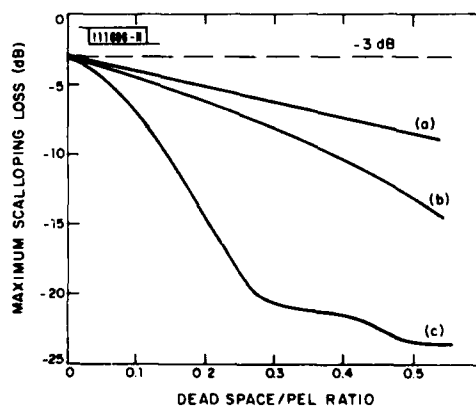
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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report covers in detail the solid state research work of the Solid State Division at Lincoln Laboratory for the period 1 May through 31 July 1981. The topics covered are Solid State Device Research, Quantum Electronics, Materials Research, Microelectronics, and Analog Device Technology. Funding is primarily provided by the Air Force, with additional support provided by the Army, DARPA, Navy, NASA, and DOE.

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